



EECS151/251A

Spring 2018

Digital Design and Integrated Circuits

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Lecture 20: Adders

Outline

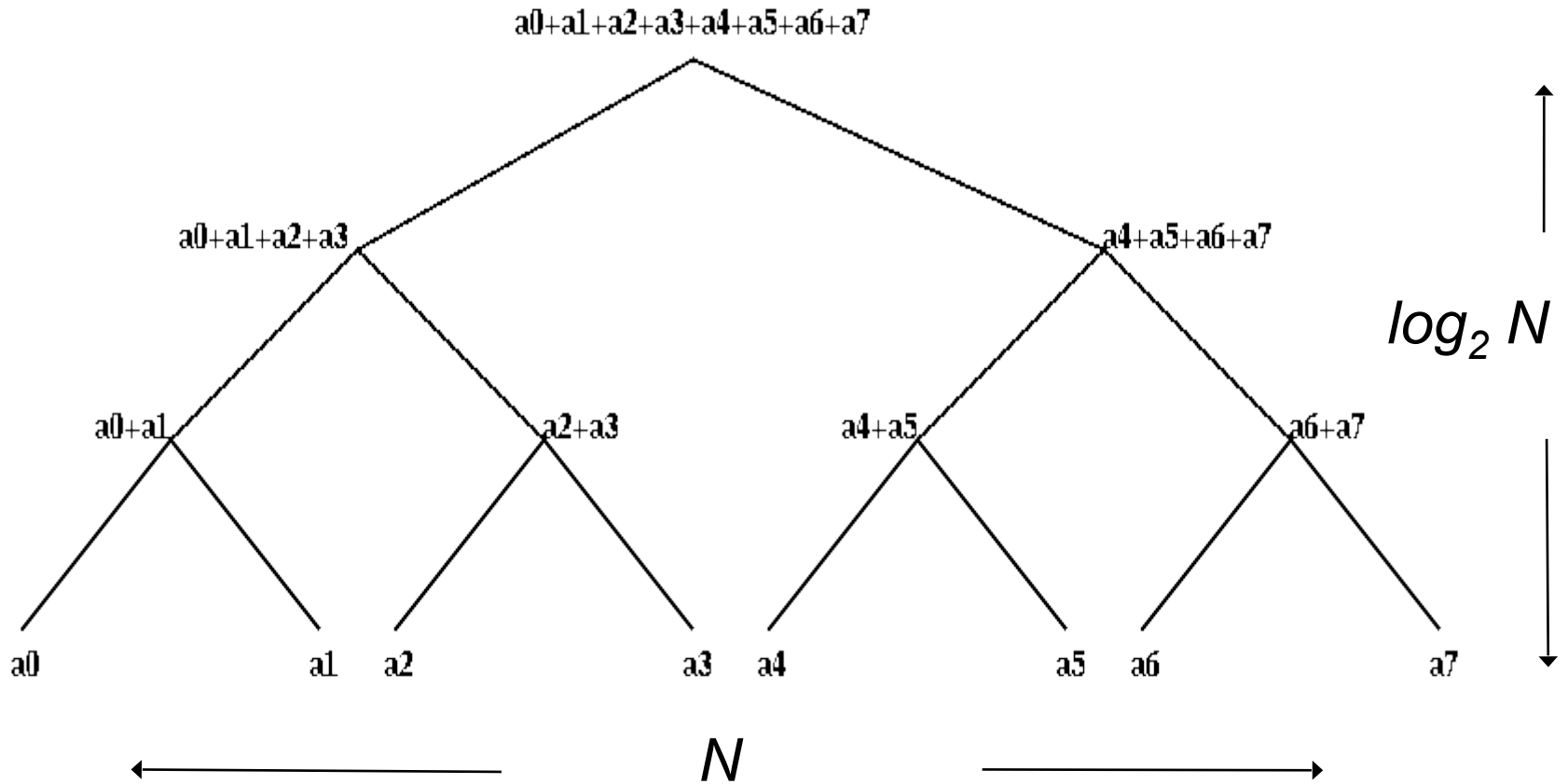


- ❑ *“tricks with trees”*
- ❑ *Adder review, subtraction, carry-select*
- ❑ *Carry-lookahead*
- ❑ *Bit-serial addition, summary*



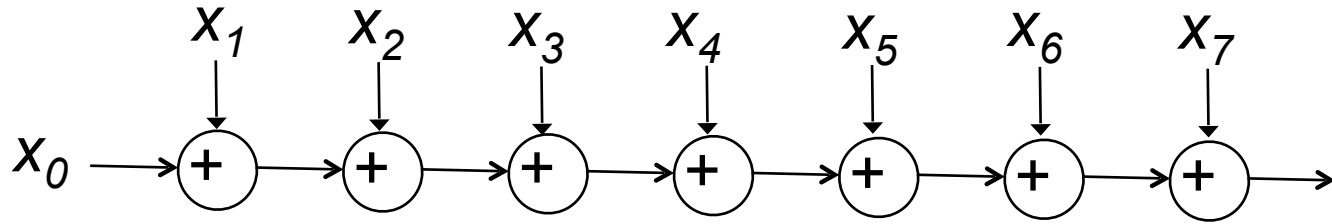
Tricks with Trees

Reductions with Trees



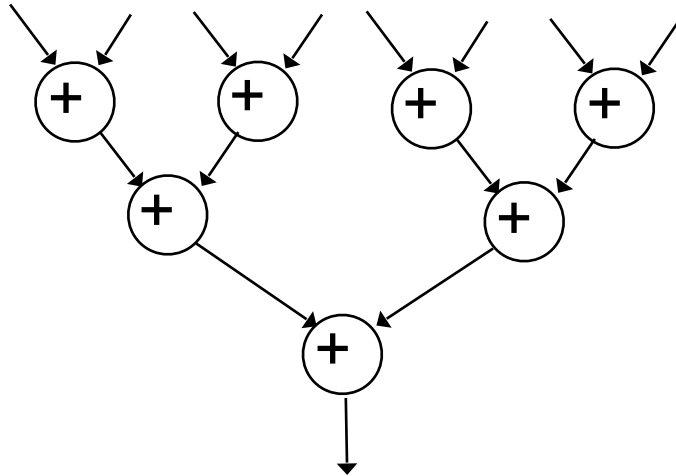
If each node (operator) is k -ary instead of binary, what is the delay?

Trees for optimization



$$T = O(N)$$

$$(((((((X_0 + X_1) + X_2) + X_3) + X_4) + X_5) + X_6) + X_7)$$



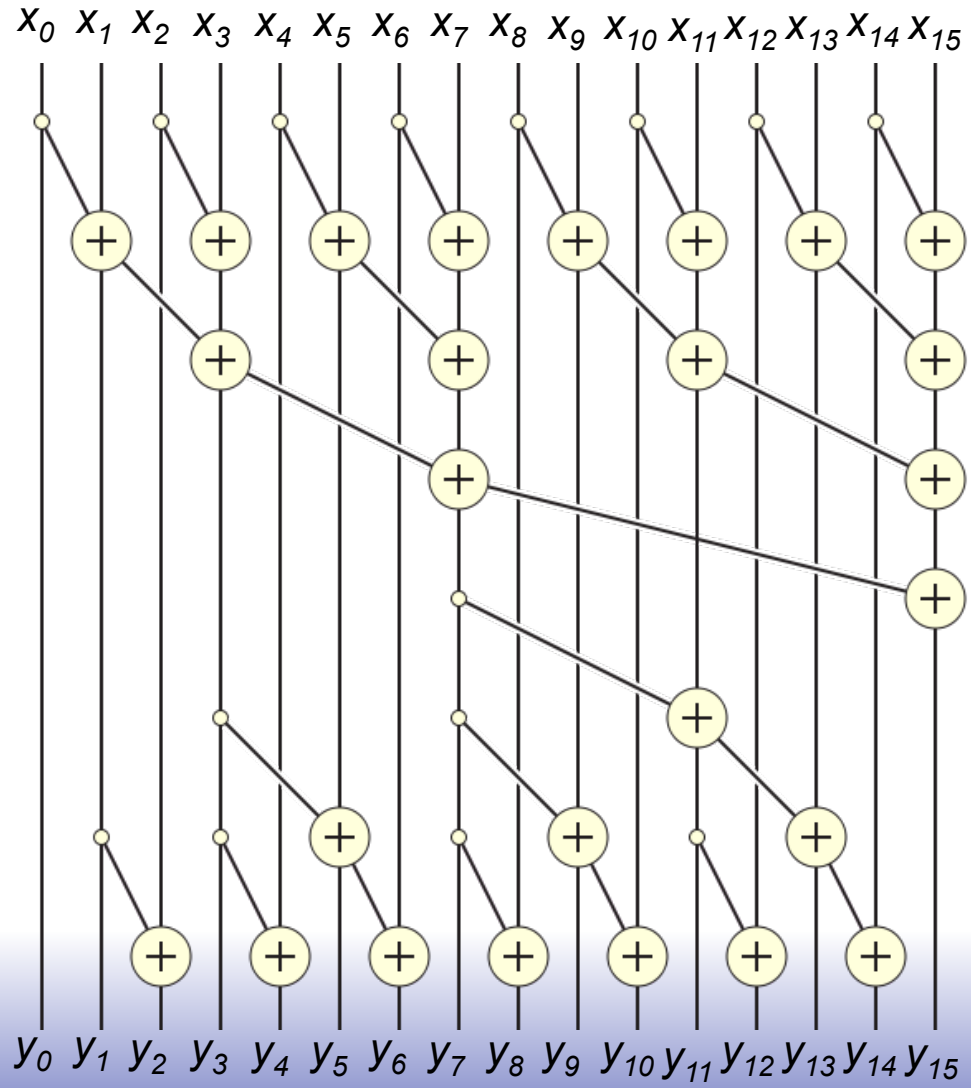
$$T = O(\log N)$$

$$((X_0 + X_1) + (X_2 + X_3)) + ((X_4 + X_5) + (X_6 + X_7))$$

- What property of “+” are we exploiting?
- Other associate operators? Boolean operations? Division? Min/Max?

Parallel Prefix, or "Scan"

- If "+" is an associative operator, and x_0, \dots, x_{p-1} are input data then parallel prefix operation computes: $y_j = x_0 + x_1 + \dots + x_j$ for $j=0, 1, \dots, p-1$





*Adder review,
subtraction, carry-select*

4-bit Adder Example

- Motivate the adder circuit design by hand addition:

$$\begin{array}{r}
 a_3 \ a_2 \ a_1 \ a_0 \\
 + \ b_3 \ b_2 \ b_1 \ b_0 \\
 \hline
 c \ r_3 \ r_2 \ r_1 \ r_0
 \end{array}$$

- Add a_0 and b_0 as follows:

| a | b | r | c |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

carry to next stage

$$r = a \text{ XOR } b = a \oplus b$$

$$c = a \text{ AND } b = ab$$

$$\begin{array}{r}
 a_3 \ a_2 \ a_1 \ a_0 \\
 + \ b_3 \ b_2 \ b_1 \ b_0 \\
 \hline
 c \ r_3 \ r_2 \ r_1 \ r_0
 \end{array}$$

- Add a_1 and b_1 as follows:

| c_i | a | b | r | co |
|-------|---|---|---|------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

$$r = a \oplus b \oplus c_i$$

$$co = ab + ac_i + bc_i$$

Algebraic Proof of Carry Simplification

$$\begin{aligned} \text{Cout} &= a'bc + ab'c + abc' + abc \\ &= a'bc + ab'c + abc' + abc + abc \\ &= a'bc + abc + ab'c + abc' + abc \\ &= (a' + a)bc + ab'c + abc' + abc \\ &= (1)bc + ab'c + abc' + abc \\ &= bc + ab'c + abc' + abc + abc \\ &= bc + ab'c + abc + abc' + abc \\ &= bc + a(b' + b)c + abc' + abc \\ &= bc + a(1)c + abc' + abc \\ &= bc + ac + ab(c' + c) \\ &= bc + ac + ab(1) \\ &= bc + ac + ab \end{aligned}$$

| | ab | | | |
|---|----|----|----|----|
| c | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |

$$\text{cout} = ab + bc + ac$$

4-bit Adder Example

Gate Representation of FA-cell

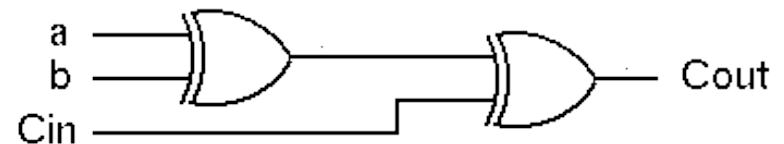
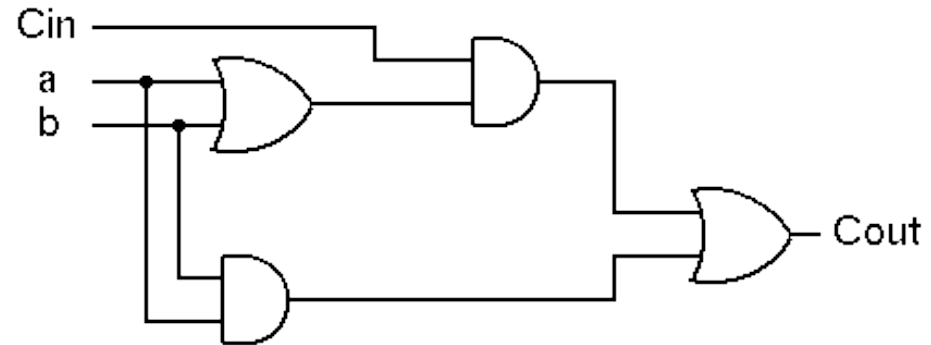
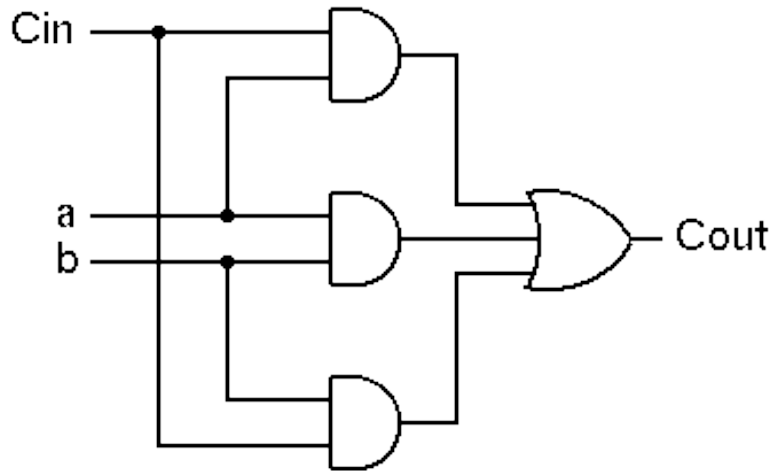
$$r_i = a_i \oplus b_i \oplus c_{in}$$

$$c_{out} = a_i c_{in} + a_i b_i + b_i c_{in}$$

- Alternative Implementation (with 2-input gates):

$$r_i = (a_i \oplus b_i) \oplus c_{in}$$

$$c_{out} = c_{in}(a_i + b_i) + a_i b_i$$

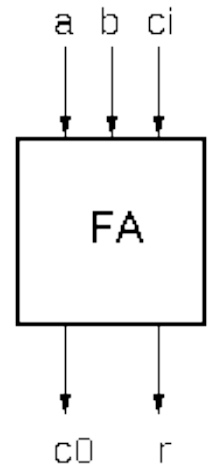


Carry-ripple Adder Revisited

□ Each cell:

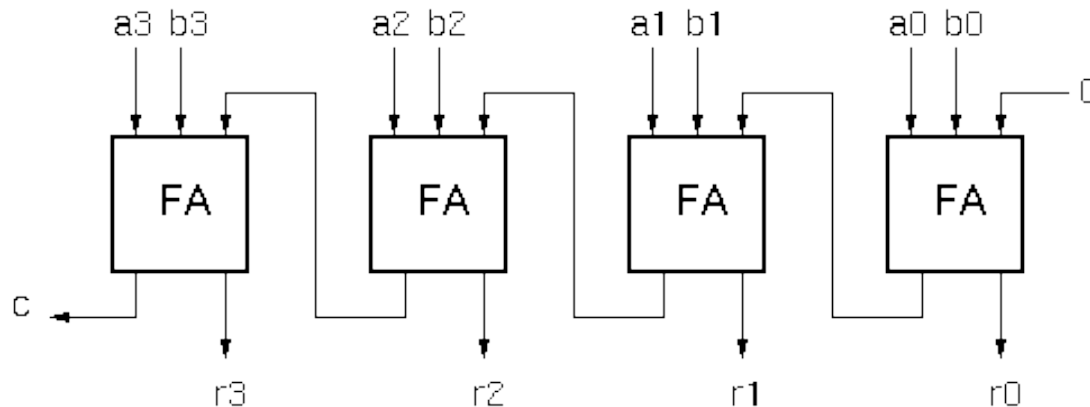
$$r_i = a_i \oplus b_i \oplus c_{in}$$

$$c_{out} = a_i c_{in} + a_i b_i + b_i c_{in} = c_{in}(a_i + b_i) + a_i b_i$$



“Full adder cell”

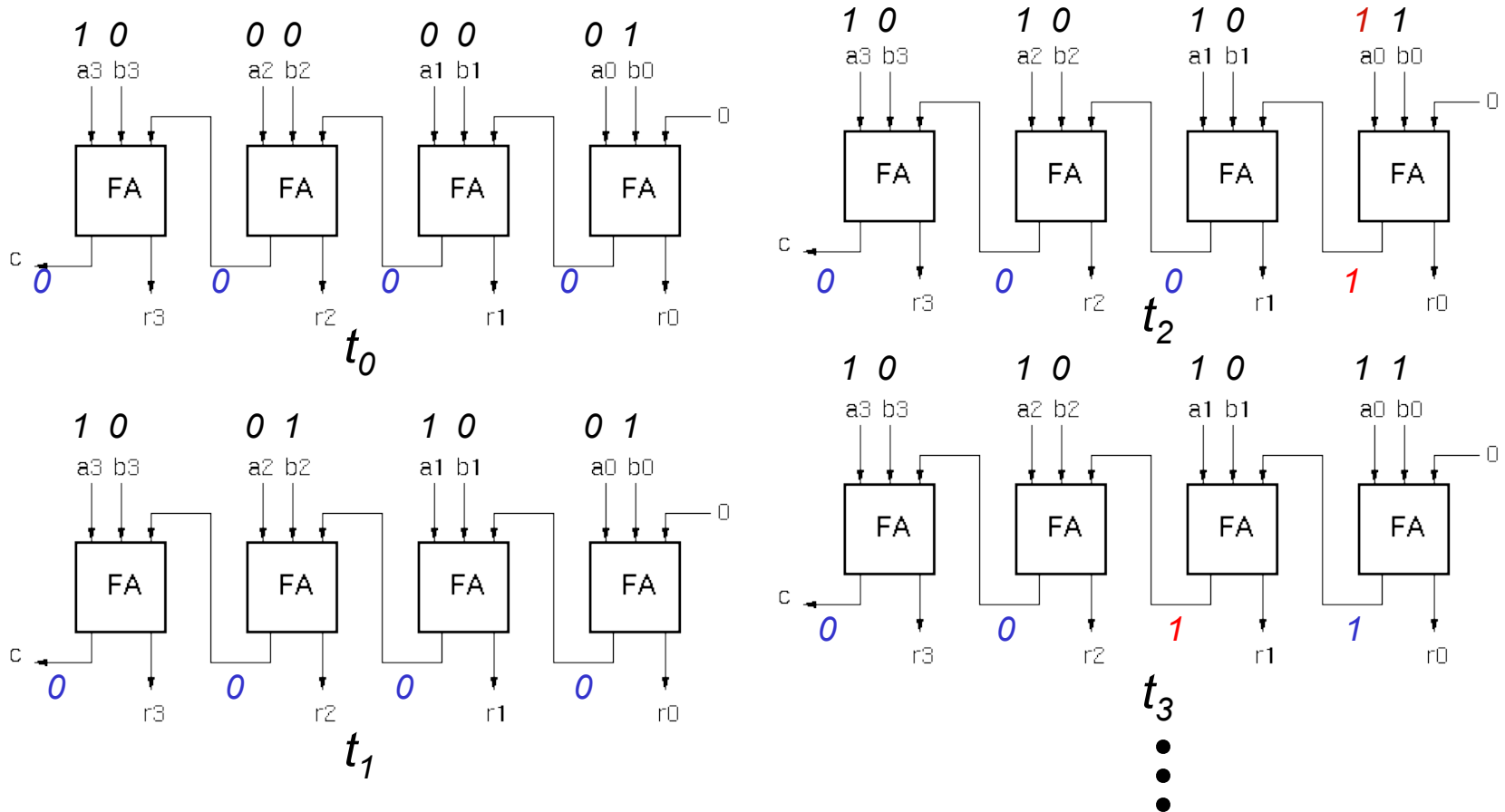
□ 4-bit adder:



□ What about subtraction?

Delay in Ripple Adders

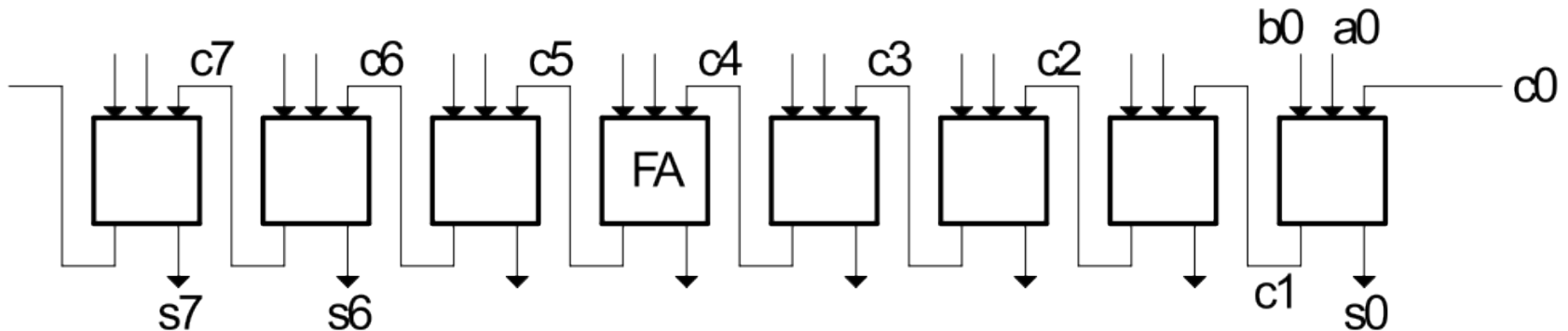
- Ripple delay amount is a function of the data inputs:



- However, we usually only consider the worst case delay on the critical path. There is always at least one set of input data that exposes the worst case delay.

Adders (cont.)

Ripple Adder

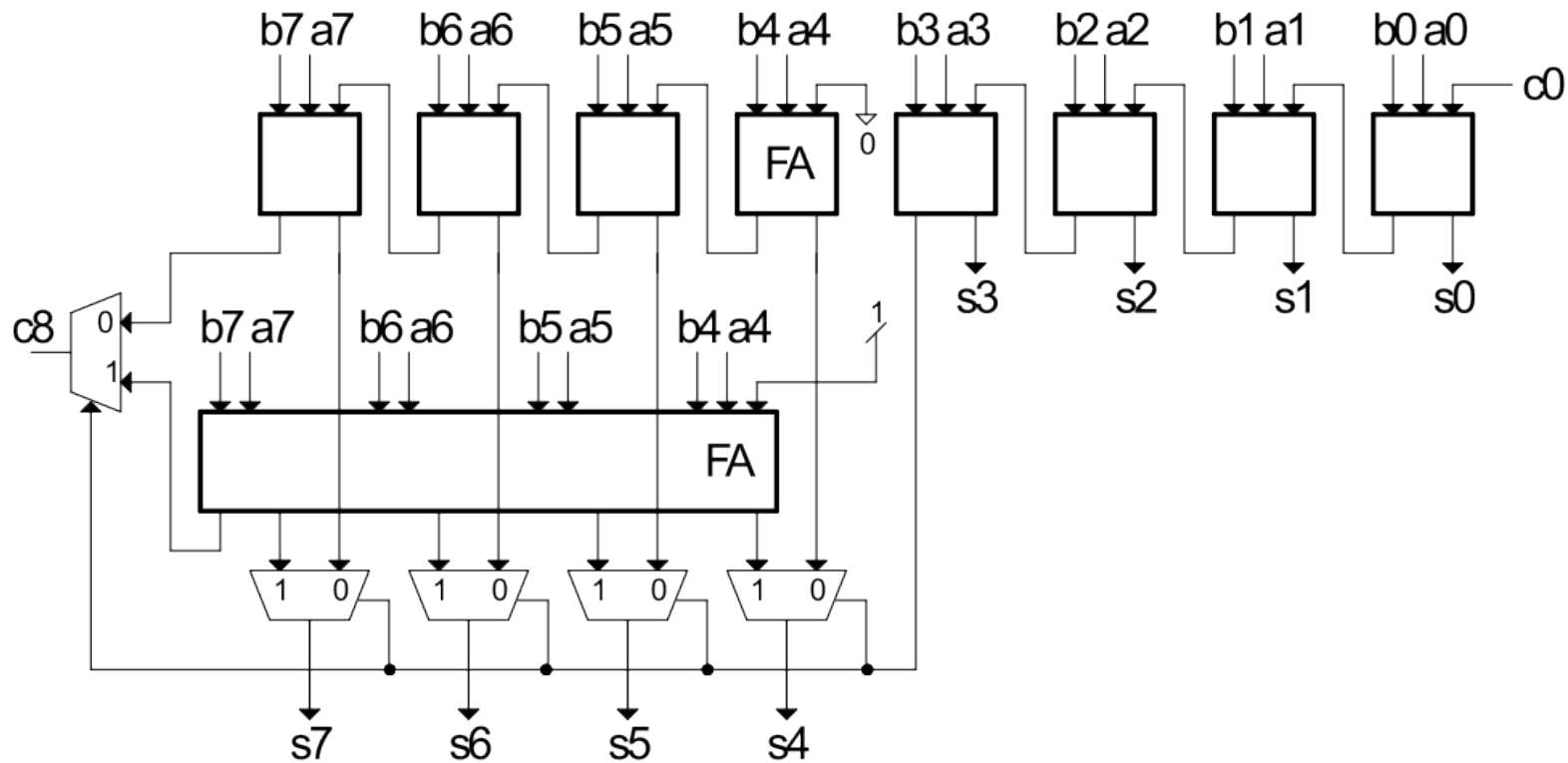


Ripple adder is inherently slow because, in worst case s_7 must wait for c_7 which must wait for c_6 ...

$$T \propto n, \text{ Cost} \propto n$$

How do we make it faster, perhaps with more cost?

Carry Select Adder

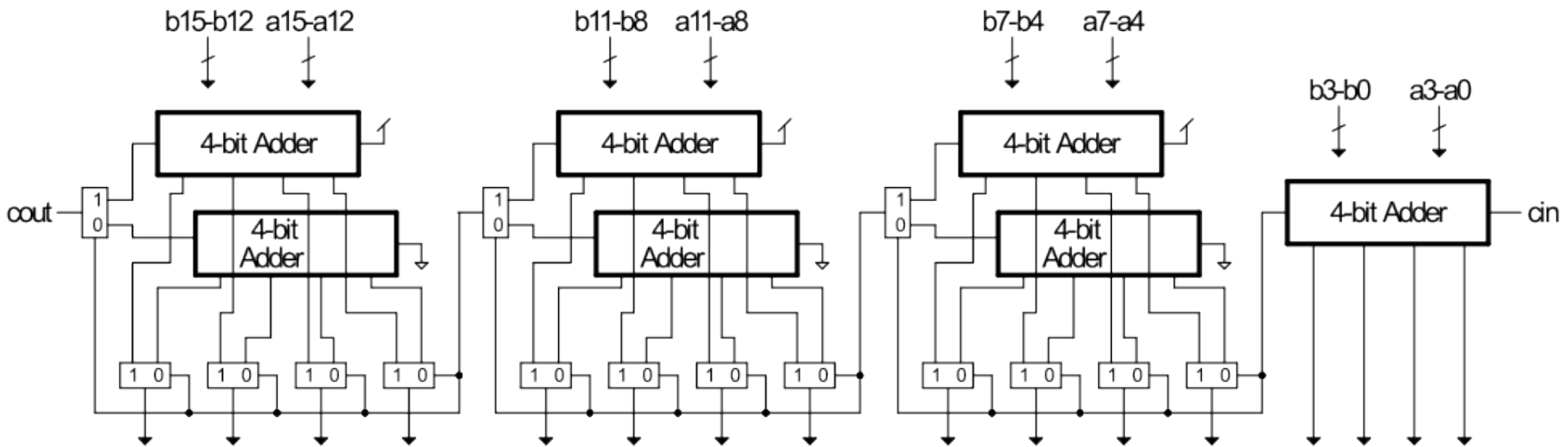


$$T = T_{ripple_adder} / 2 + T_{MUX}$$

$$COST = 1.5 * COST_{ripple_adder} + (n/2 + 1) * COST_{MUX}$$

Carry Select Adder

Extending Carry-select to multiple blocks



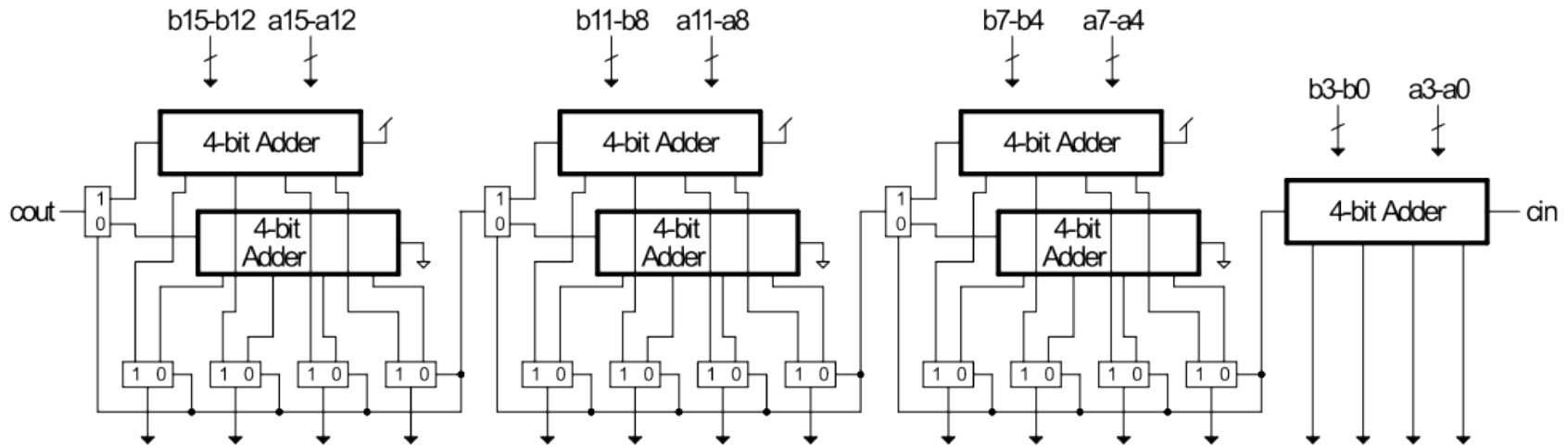
What is the optimal # of blocks and # of bits/block?

- If blocks too small delay dominated by total mux delay
- If blocks too large delay dominated by adder ripple delay

\sqrt{N} stages of \sqrt{N} bits

$T \propto \text{sqrt}(N)$,
 $\text{Cost} \approx 2 * \text{ripple} + \text{muxes}$

Carry Select Adder



- Compare to ripple adder delay:

$$T_{total} = 2 \sqrt{N} T_{FA} - T_{FA}, \text{ assuming } T_{FA} = T_{MUX}$$

$$\text{For ripple adder } T_{total} = N T_{FA}$$

“cross-over” at N=3, Carry select faster for any value of N>3.

- Is \sqrt{N} really the optimum?

- From right to left increase size of each block to better match delays
- Ex: 64-bit adder, use block sizes [12 11 10 9 8 7 7], the exact answer depends on the relative delay of mux and FA



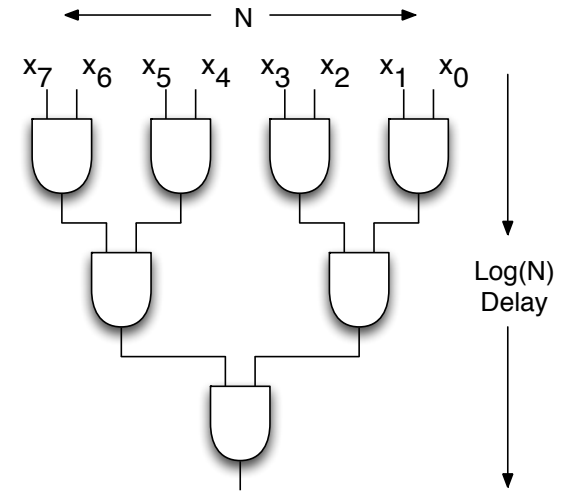
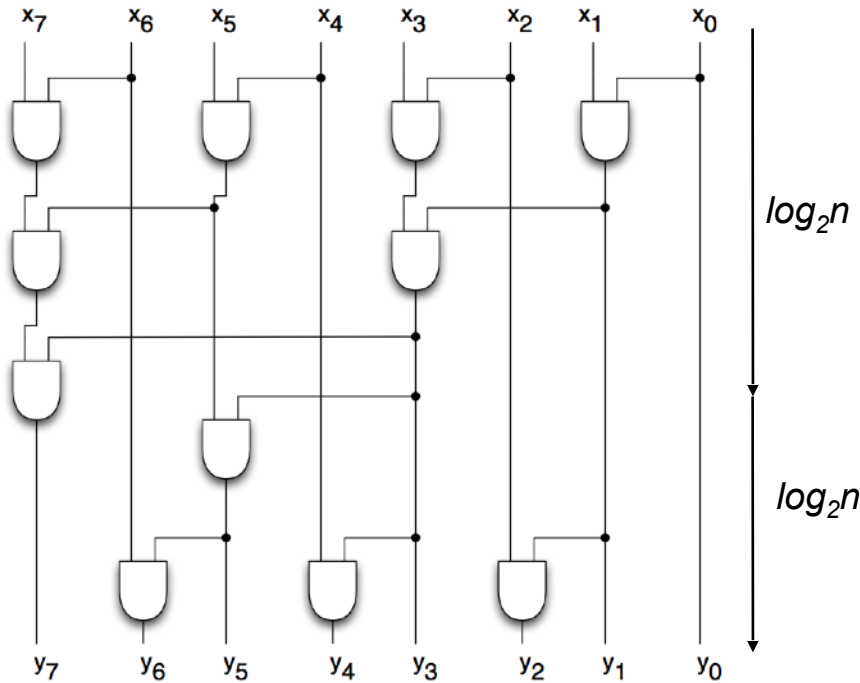
*Carry-lookahead and
Parallel Prefix*

Adders with Delay $\propto \log(n)$

Can carry generation be made to be a kind of “reduction operation”?

Lowest delay for a reduction is a balanced tree.

- *But in this case all intermediate values are required.*
- *One way is to use “Parallel Prefix” to compute the carries.*



$$y_0 = x_0$$

$$y_1 = x_0x_1$$

$$y_2 = x_0x_1x_2$$

Carry Look-ahead Adders

- How do we arrange carry generation to be associative?
- Reformulate basic adder stage:

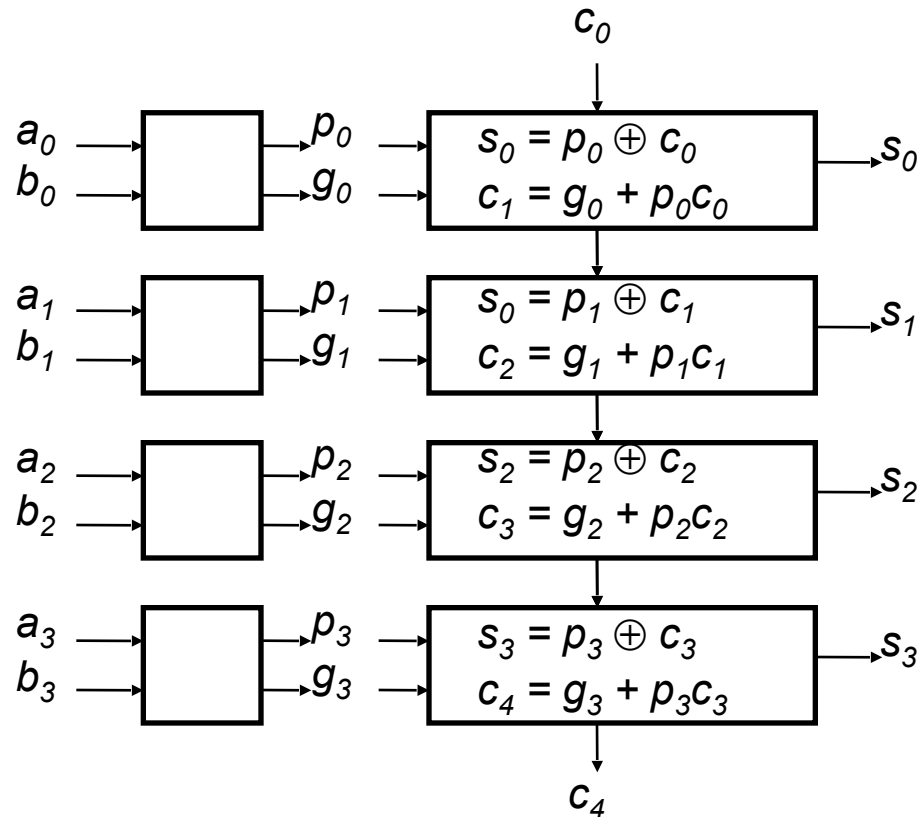
| a | b | c_i | c_{i+1} | s | |
|-----|-----|-------|-----------|-----|--------------------------|
| 0 | 0 | 0 | 0 | 0 | <i>carry "kill"</i> |
| 0 | 0 | 1 | 0 | 1 | $k_i = a_i' b_i'$ |
| 0 | 1 | 0 | 0 | 1 | |
| 0 | 1 | 1 | 1 | 0 | <i>carry "propagate"</i> |
| 1 | 0 | 0 | 0 | 1 | $p_i = a_i \oplus b_i$ |
| 1 | 0 | 1 | 1 | 0 | |
| 1 | 1 | 0 | 1 | 0 | <i>carry "generate"</i> |
| 1 | 1 | 1 | 1 | 1 | $g_i = a_i b_i$ |

$$c_{i+1} = g_i + p_i c_i$$
$$s_i = p_i \oplus c_i$$

Carry Look-ahead Adders

- Ripple adder using p and g signals:

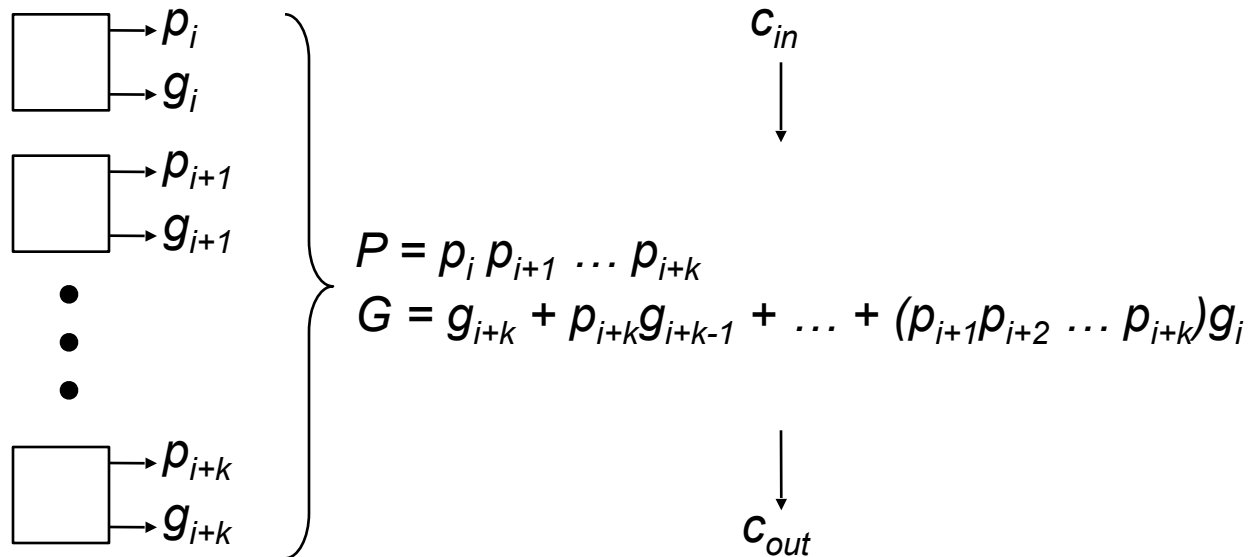
$$p_i = a_i \oplus b_i$$
$$g_i = a_i b_i$$



- So far, no advantage over ripple adder: $T \propto N$

Carry Look-ahead Adders

- “Group” propagate and generate signals:

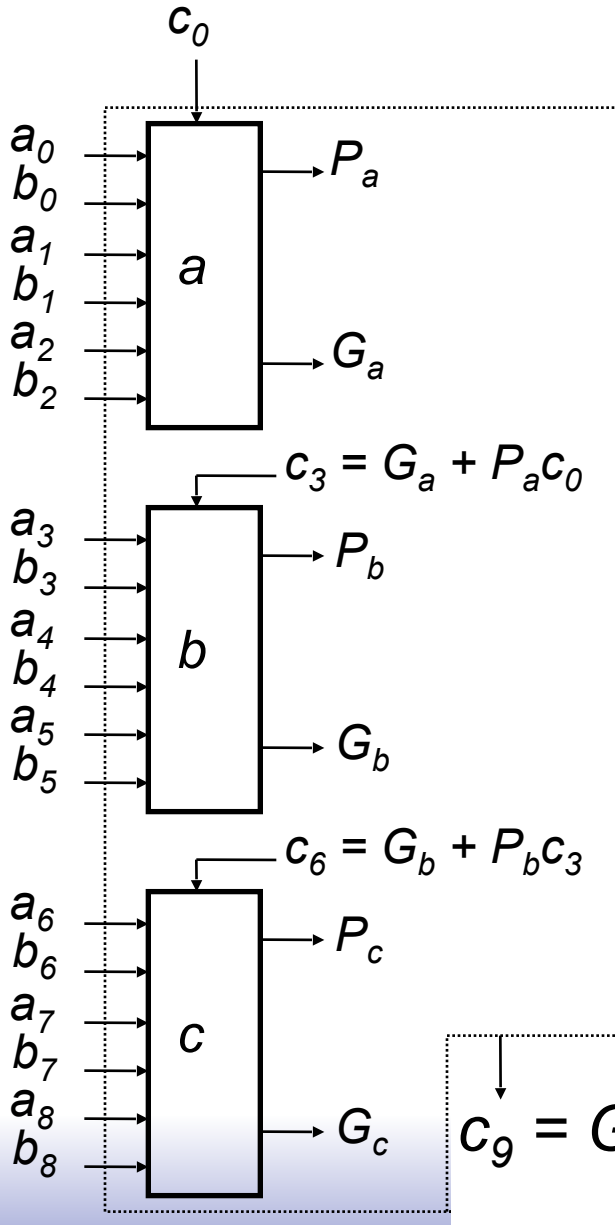


- P true if the group as a whole propagates a carry to c_{out}
- G true if the group as a whole generates a carry

$$c_{out} = G + P c_{in}$$

- Group P and G can be generated hierarchically.

Carry Look-ahead Adders

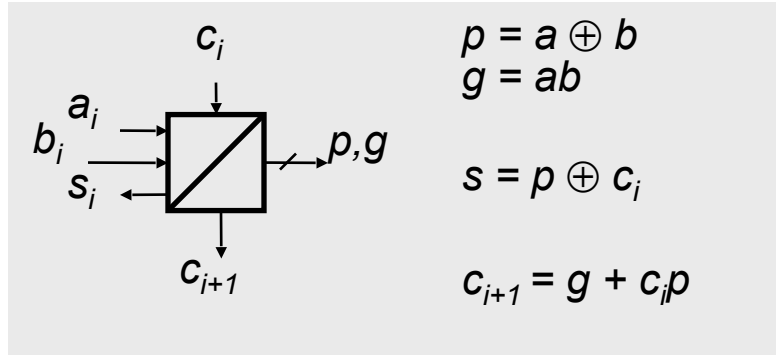
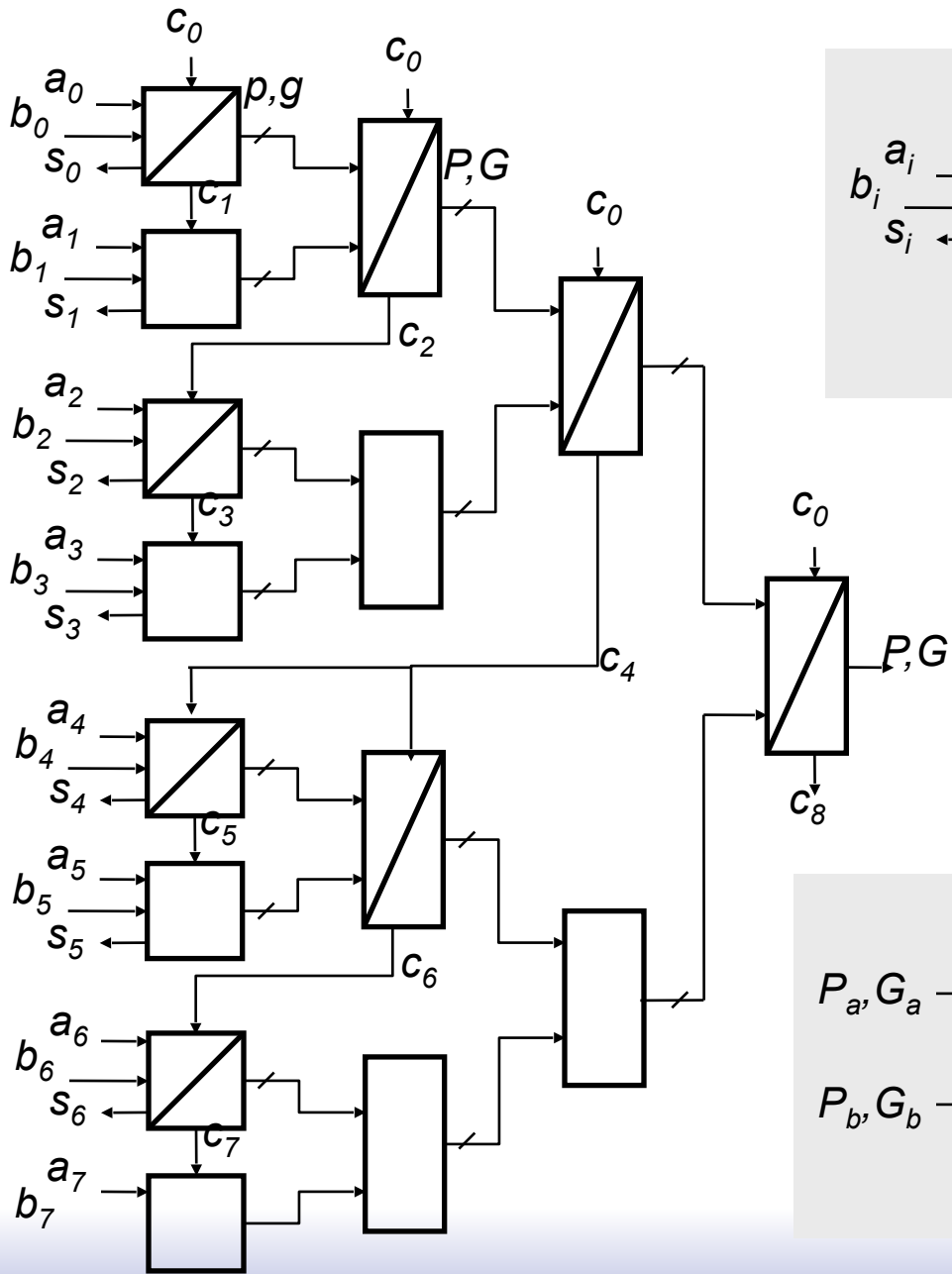


9-bit Example of hierarchically generated P and G signals:

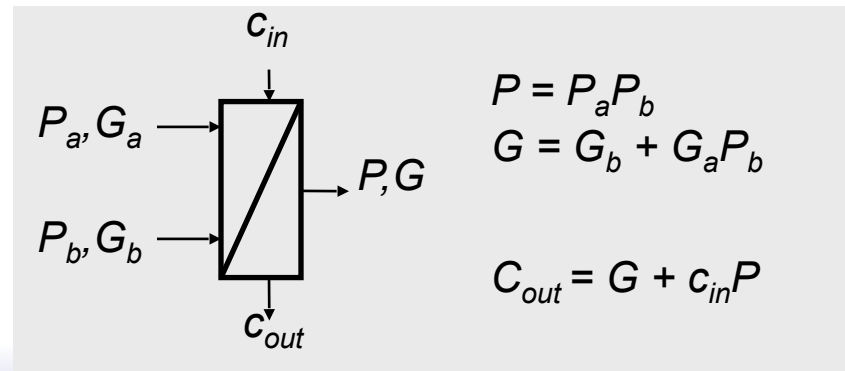
$$P = P_a P_b P_c$$

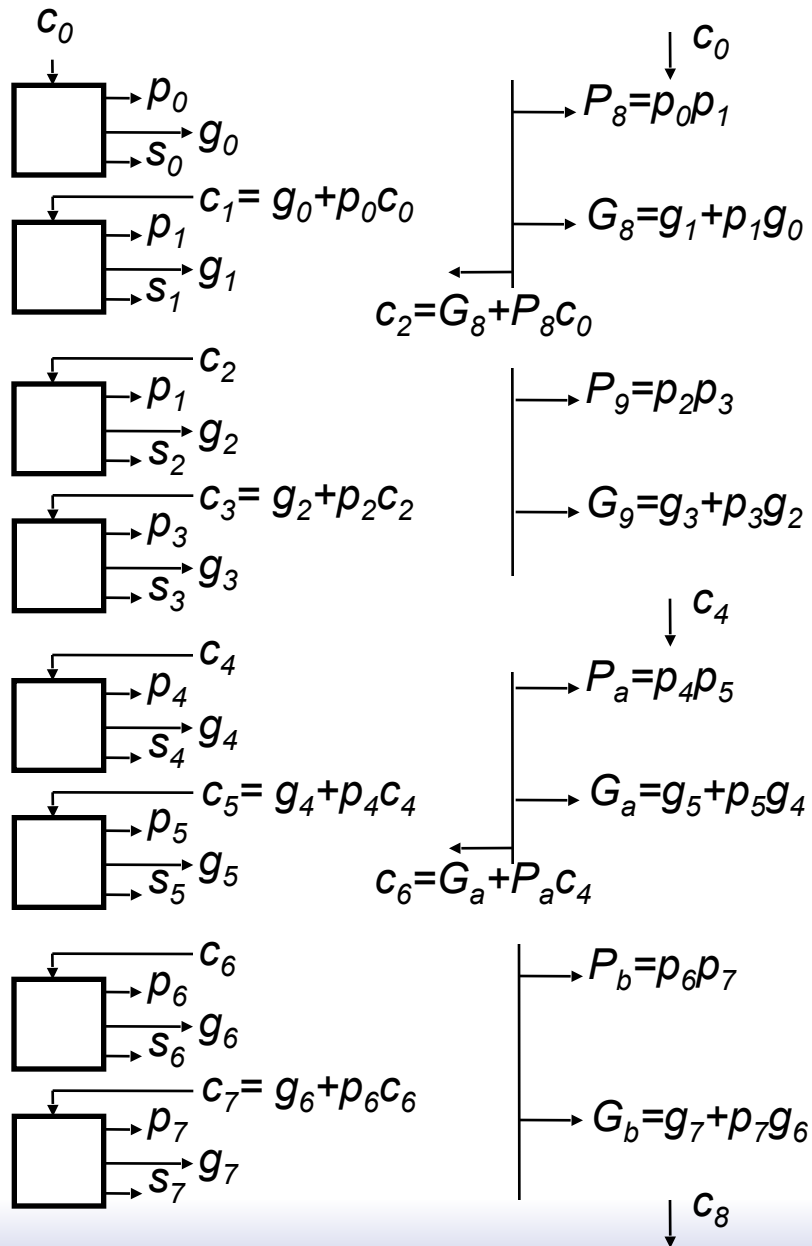
$$G = G_c + P_c G_b + P_b P_c G_a$$

$$c_9 = G + P c_0$$

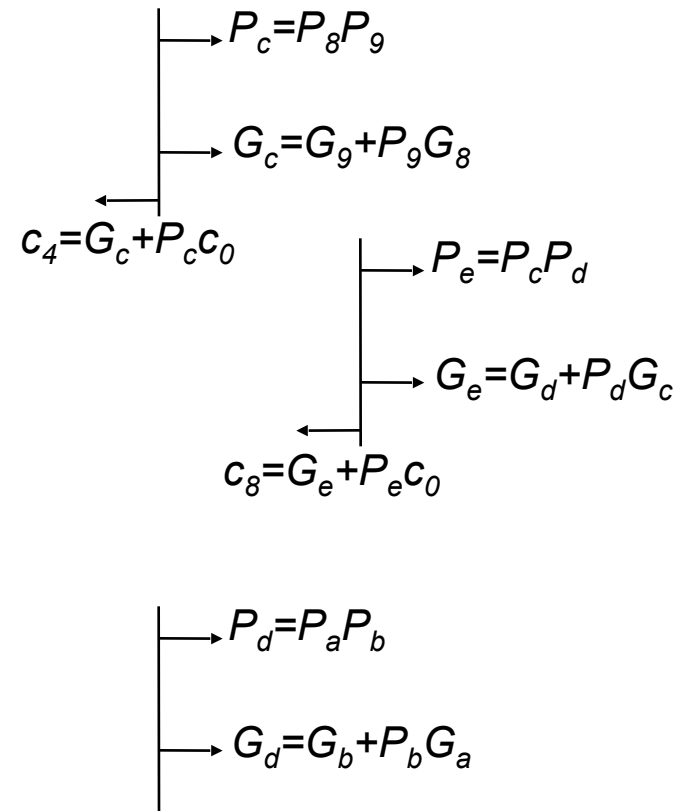


8-bit Carry Look-ahead Adder





8-bit Carry Look-ahead Adder with 2-input gates.



Parallel-Prefix Carry Look-ahead Adders

- Generate all carries directly (no grouping):

$$c_0 = 0$$

$$c_1 = g_0 + p_0 c_0 = g_0$$

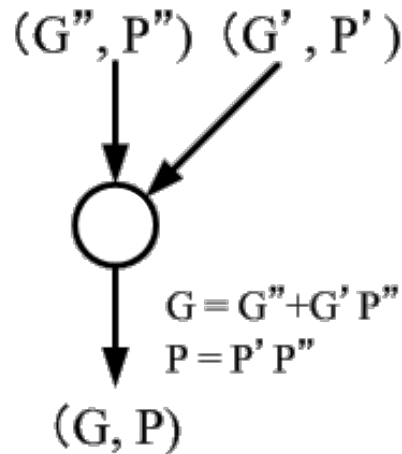
$$c_2 = g_1 + p_1 c_1 = g_1 + p_1 g_0$$

$$c_3 = g_2 + p_2 c_2 = g_2 + p_2 g_1 + p_1 p_2 g_0$$

$$c_4 = g_3 + p_3 c_3 = g_3 + p_3 g_2 + p_3 p_2 g_1 + p_4 p_3 p_2 g_0$$

⋮
⋮
⋮

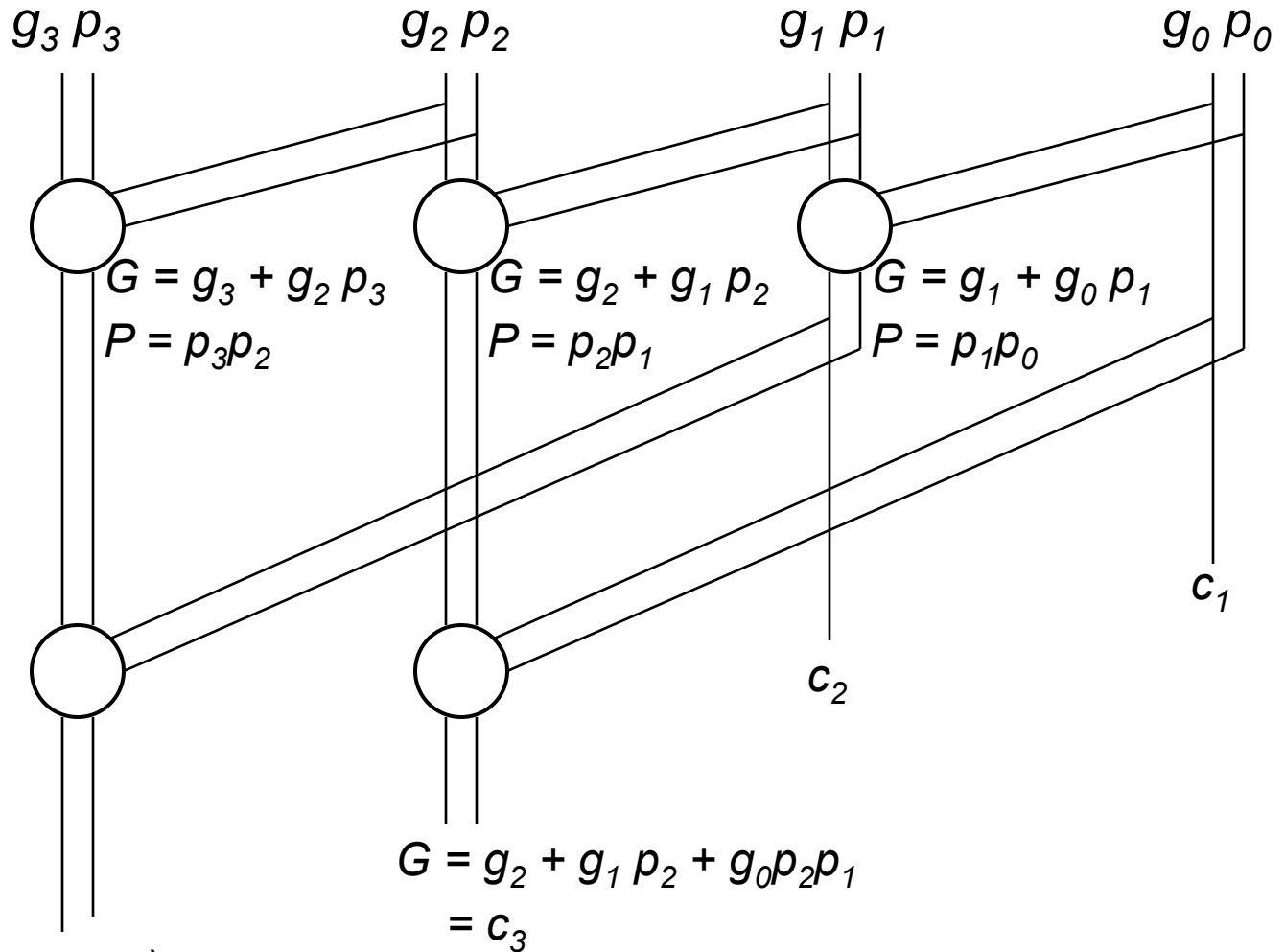
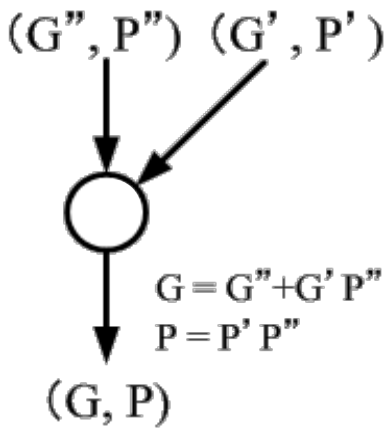
$$c_{i+1} = g_i + p_i c_i$$



*Binary (G, P)
associative operator*

Use binary (G,P) operator to form parallel prefix tree

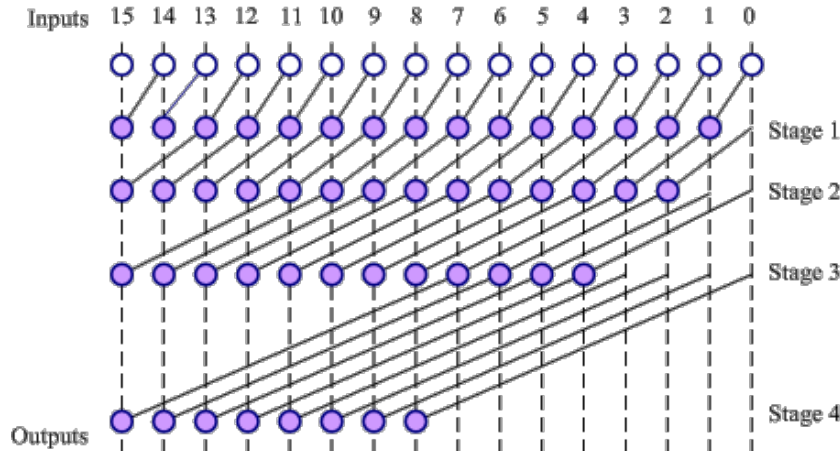
Parallel Prefix Adder Example



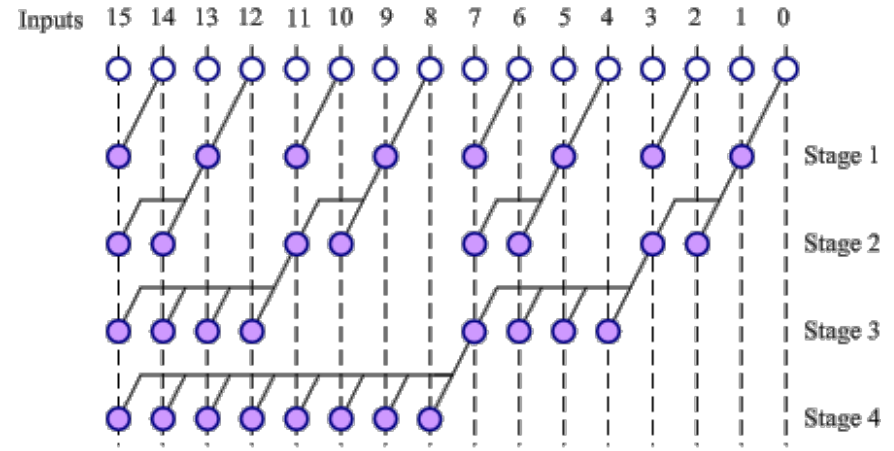
$$\begin{aligned}
 G &= g_3 + g_2 p_3 + (g_1 + g_0 p_1) p_3 p_2 \\
 &= g_3 + g_2 p_3 + g_1 p_3 p_2 + g_0 p_3 p_2 p_1 \\
 &= c_4
 \end{aligned}$$

$$s_i = a_i \oplus b_i \oplus c_i = p_i \oplus c_i$$

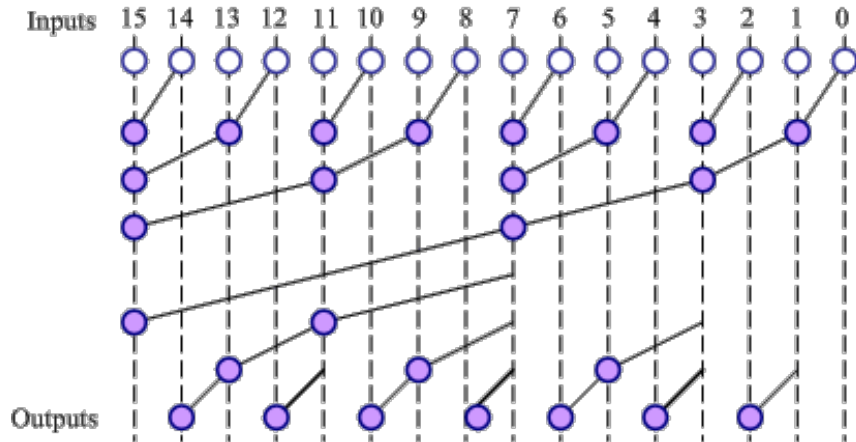
Other Parallel Prefix Adder Architectures



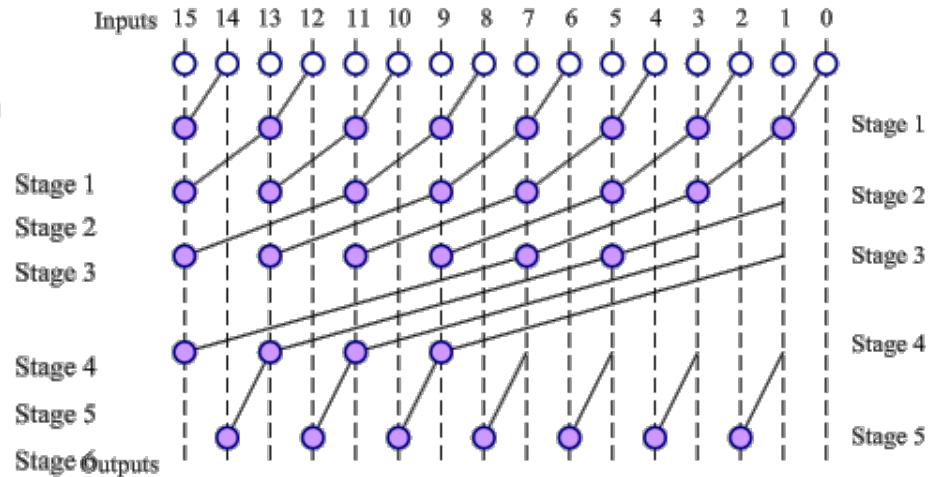
Kogge-Stone adder: minimum logic depth, and full binary tree with minimum fan-out, resulting in a fast adder but with a large area



Ladner-Fischer adder: minimum logic depth, large fan-out requirement up to $n/2$



Brent-Kung adder: minimum area, but high logic depth



Han-Carlson adder: hybrid design combining stages from the Brent-Kung and Kogge-Stone adder

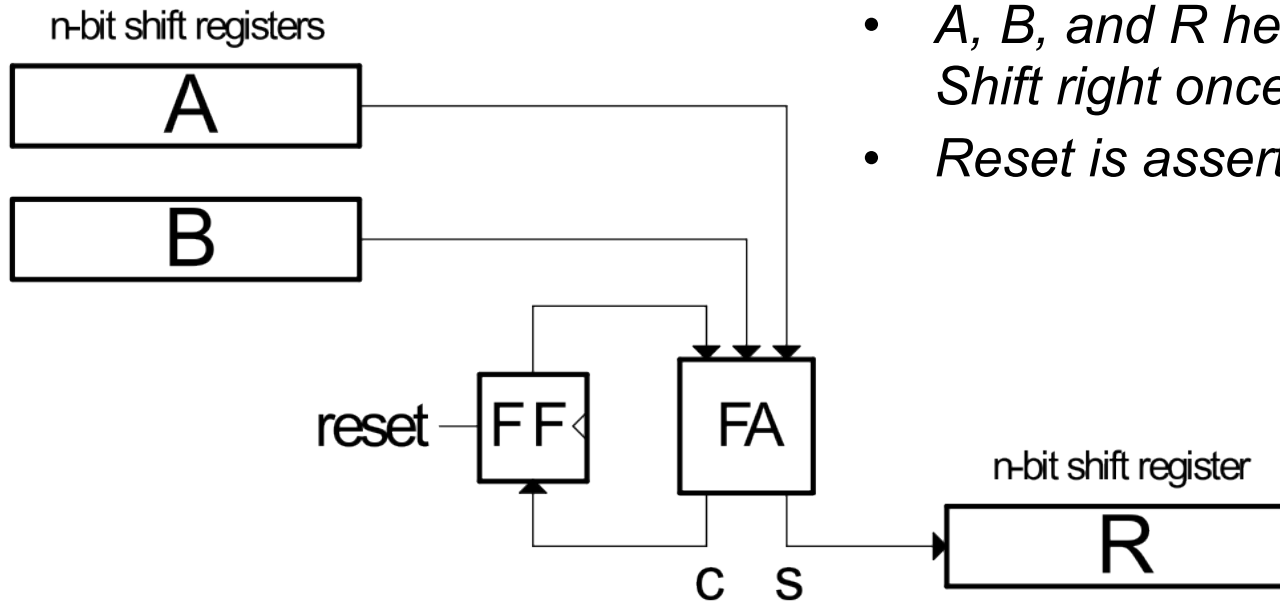
Carry look-ahead Wrap-up

- ❑ Adder delay $O(\log N)$.
- ❑ Cost?
- ❑ Can be applied with other techniques. Group P & G signals can be generated for sub-adders, but another carry propagation technique (for instance ripple) used within the group.
 - For instance on FPGA. Ripple carry up to 32 bits is fast (1.25ns), CLA used to extend to large adders. CLA tree quickly generates carry-in for upper blocks.



*Bit-serial Addition, Adder
summary*

Bit-serial Adder



- *A, B, and R held in shift-registers. Shift right once per clock cycle.*
- *Reset is asserted by controller.*

□ Addition of 2 n-bit numbers:

- takes n clock cycles,
- uses 1 FF, 1 FA cell, plus registers
- the bit streams may come from or go to other circuits, therefore the registers might not be needed.

Adder Final Words

| Type | Cost | Delay |
|-----------------|--------|---------------|
| Ripple | $O(N)$ | $O(N)$ |
| Carry-select | $O(N)$ | $O(\sqrt{N})$ |
| Carry-lookahead | $O(N)$ | $O(\log(N))$ |
| Bit-serial | $O(1)$ | $O(N)$ |

- ❑ Dynamic energy per addition for all of these is $O(n)$.
- ❑ “O” notation hides the constants. Watch out for this!
- ❑ The “real” cost of the carry-select is at least 2X the “real” cost of the ripple. “Real” cost of the CLA is probably at least 2X the “real” cost of the carry-select.
- ❑ The actual multiplicative constants depend on the implementation details and technology.
- ❑ FPGA and ASIC synthesis tools will try to choose the best adder architecture automatically - assuming you specify addition using the “+” operator, as in “`assign A = B + C`”