EECS151/251A
Spring 2018
Digital Design and Integrated Circuits

Instructors:
John Wawrzynek and Nick Weaver

Lecture 26:
Wrap-up

Outline

- *Important takeaways*
- *Digital Design – Where to from here?*

Why Study and Learn Digital Design?

- We expect that many of our graduates will eventually be employed as designers.
  - ***Digital design is not a spectator sport.*** The only way to learn it, and to appreciate the issues, is to do it.
  - To a large extent, it comes with practice/experience (this course is just the beginning).
  - Another way to get better is to study other designs. Not time to do much of this during the semester, but a good practice for later.
- However, a significant percentage of our graduates will not be digital designers. What's in it for them?
  - Better manager of designers, marketers, field engineers, etc.
  - Better researcher/scientist/designer in related areas
    - Software engineers, fabrication process development, etc.
  - To become a better user of electronic systems.

In What Context Will You be Designing?

Engineers learn so that they can build.
Scientists build so that they can learn.

- Electronic design is a critical tool for most areas of pure science:
  - Astrophysics – special electronics used for processing radio antenna signals.
  - Genomics – special processing architectures for DNA string matching.
  - In general - sensor processing, control, and number crunching. In some fields, computation has replaced experimentation – particle physics, world weather prediction (fluid dynamics).
- In computer engineering, prototypes often designed, implemented, and studied to "prove out" an idea. Common within Universities and industrial research labs. Lessons learned and proven ideas often transferred to industry through licensing, technical communications, or startup companies.
  - RISC processors were first proved out at Berkeley and IBM Research

Designs in Industry

- Of course, companies are the primary employer of designers. Provide some useful products to society or government and make a profit for the shareholders.
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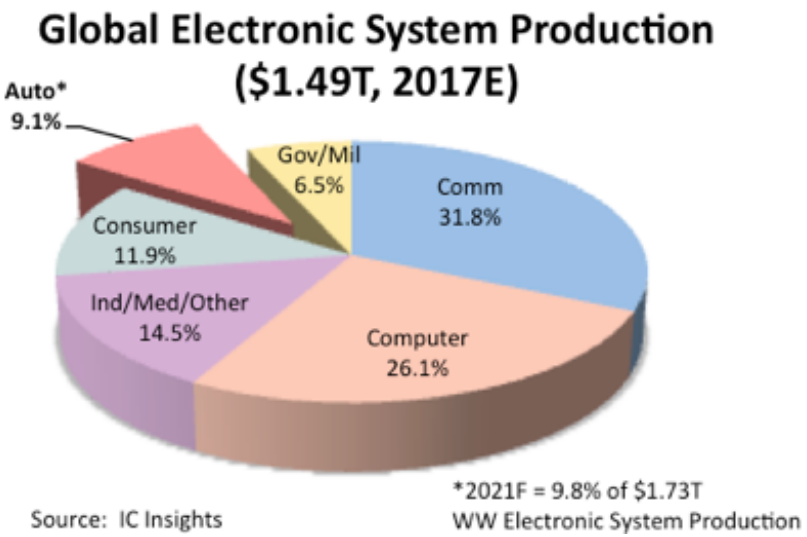
- Interesting recent shift
  - All software giants now have hardware design teams (embedded and chips)
  - Google, Amazon, Facebook, Microsoft, …



Ten Big Ideas from EECS151

1. **Modularity and Hierarchy** is an important way to describe and think about digital systems.
2. **Parallelism** is a key property of hardware systems and distinguishes them from serial software execution.
3. **Clocking** and the use of state elements (latches, flip-flops, and memories) control the flow of data.
4. **Cost/Performance/Power tradeoffs** are possible at all levels of the system design.
5. **Boolean Algebra** and other logic representations.
6. Hardware Description Languages **(HDLs) and Logic Synthesis** are a central tool for digital design.
7. **Datapath + Controller** is a effective design pattern.
8. **Finite State Machines** abstraction gives us a way to model any digital system – used for designing controllers.
9. **Arithmetic circuits** are often based on “long-hand” arithmetic techniques.
10. **FPGAs + ASICs** give us a convenient and flexible implementation technology.

What We Didn't Cover

- Design Verification and Testing
  - Industrial designers spend more than half their time testing and verifying correctness of their designs.
    - Some of this covered in the lab and a bit in lecture. Didn't cover rigorous testing procedures and "formal verification".
  - Most industrial products are designed from the start for testability. Important for design verification and later for manufacturing test.
  - Related: Design for Test, Fault modeling and fault tolerant design.
- Other High-level Optimization Techniques
  - Ex: Automatic Retiming (although CAD tools do it)
  - High-level Synthesis - now starting to catch on
- Other High-level Architectures: GPUs, video processing, network routers, …
- Asynchronous Design

Most Closely Related Courses

- CS152 Computer Architecture and Engineering
  - Design and Analysis of Microprocessors
  - Applies basic design concepts from EECS151
- EE241B Digital Integrated Circuits
  - Transistor-level design of ICs
  - More on Advanced ASIC Tool use
- CS250 VLSI Systems Design
  - Advanced-undergrad/grad course
  - Design tradeoffs at the chip design level

Future Design Issues

- Automatic High-level synthesis (HLS) and optimization (with micro-architecture synthesis) and hardware/software co-design.
- Current trend is towards “system on a chip” (SOC) design methodology:
  - Pre-designed subsystems (processor cores, bus controllers, memory systems, network interfaces, etc.) connected with standard on-chip interconnect or bus.
  - Strong emphasis on “accelerators”.
- Increasing NREs will favor post-fabrication customization.
- A number of alternatives to silicon VLSI have been proposed, including techniques based on:
  - Carbon nanotubes*, molecular electronics, quantum mechanics, and biological processes.
  - How will these change the way we design systems?

*In 2012, IBM produced a sub-10 nm carbon nanotube transistor that outperformed silicon on speed and power. "The superior low-voltage performance of the sub-10 nm CNT transistor proves the viability of nanotubes for consideration in future aggressively scaled transistor technologies", according to the abstract of the paper in Nano Letters.

Important Topics for Final Exam

(More comprehensive, detailed list later.)

1. Design problems - RTL level design with optimizations
2. Boolean algebra, K-maps, FSM design
3. Circuit timing with logical Effort
4. Arithmetic block design with performance/cost trade-offs (Adders and Multipliers)
5. Energy and power in CMOS (circuit and block level)
6. DRAM or SRAM internal operation and composition (including caches & FIFOs)
7. Synchronous design timing (pipelines, clock uncertainty)
8. Physical design (wire delay, clock distribution, power distribution)

Digital Design - Where does it go from here?

Technology Outlook

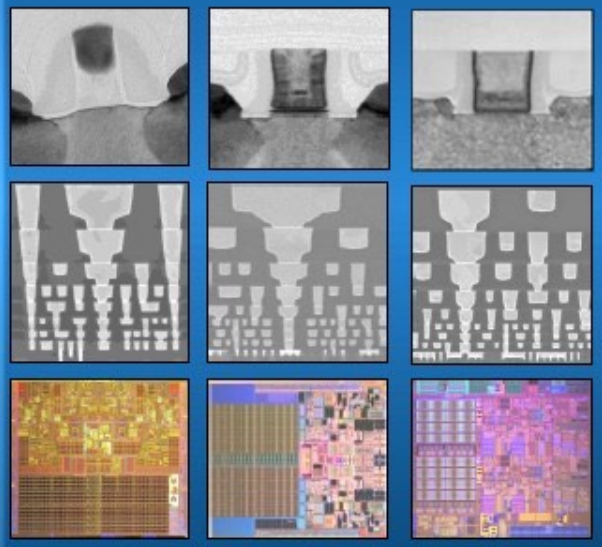
High Volume Manufacturing	2008	2010	2012	2014	2016	2018	2020	2022
Technology Node (nm)	45	32	22	16	11	8	6	4
Integration Capacity (BT)	8	16	32	64	128	256	512	1024
Delay Scaling	>0.7			~1?				
Energy Scaling	~0.5			>0.5				
Transistors	Planar			3D, FinFET				
Variability	High			Extreme				
ILD	~3			towards 2				
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	8-9	0.5 to 1 Layer per generation						

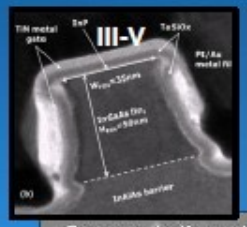
THE OPTIMISTIC PERSPECTIVE

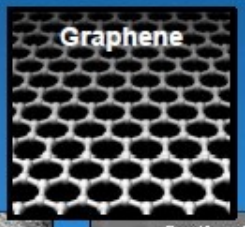
Innovation-Enabled Technology Pipeline is Full

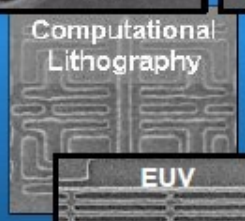
65nm	45nm	32nm	22nm	14nm	10nm	7nm	5nm	Beyond ...
2005	2007	2009	2011	2013	2015	2017	2019	2021+

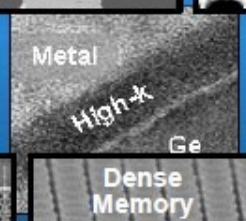
MANUFACTURING → DEVELOPMENT → RESEARCH

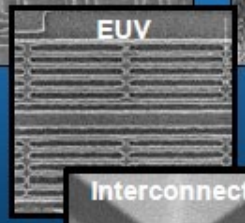


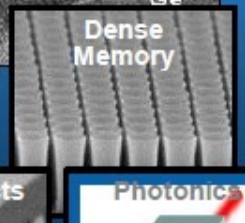


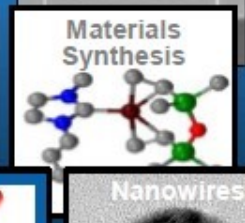


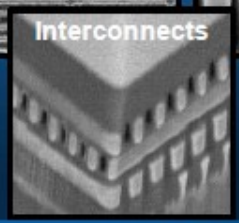


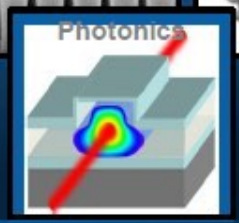


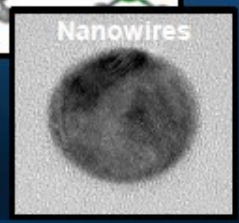












Our limit to visibility goes out ~10 years

Where are we at? Between 10 and 7nm

From Wikipedia

Oct 2016, Samsung Electronics announced mass production at 10 nm.

Q1 2017, Intel and foundries at TSMC and Samsung begin volume production of 10 nm devices, with foundry customers for 2017 including Qualcomm (Snapdragon 835) at Samsung, and Apple Inc. and MediaTek at TSMC.

April 2017, Samsung started shipping their Galaxy S8 smartphone which uses the company's version of the 10 nm processor.

June 2017, Apple delivered second-generation iPad Pro tablets powered with TSMC-produced Apple A10X chips using the 10 nm FinFET process.

Sep 2017, Apple announced the Apple A11, a 64-bit ARM-based system on a chip, manufactured by TSMC using a 10 nm FinFET process and containing 4.3 billion transistors on a die 87.66 square mm

Early 2017, TSMC had produced 256 Mbit SRAM cells at their 7 nm process with a cell area of 0.027 μm^2 (550 F^2) with reasonable risk production yields.

First half of 2017, TSMC begins 7 nm trial production. TSMC announces to begins 7 nm risk production in June 2018.

Sep 2016, GlobalFoundries announced trial production in the second half of 2017 and risk production in early 2018, with test chips already running.

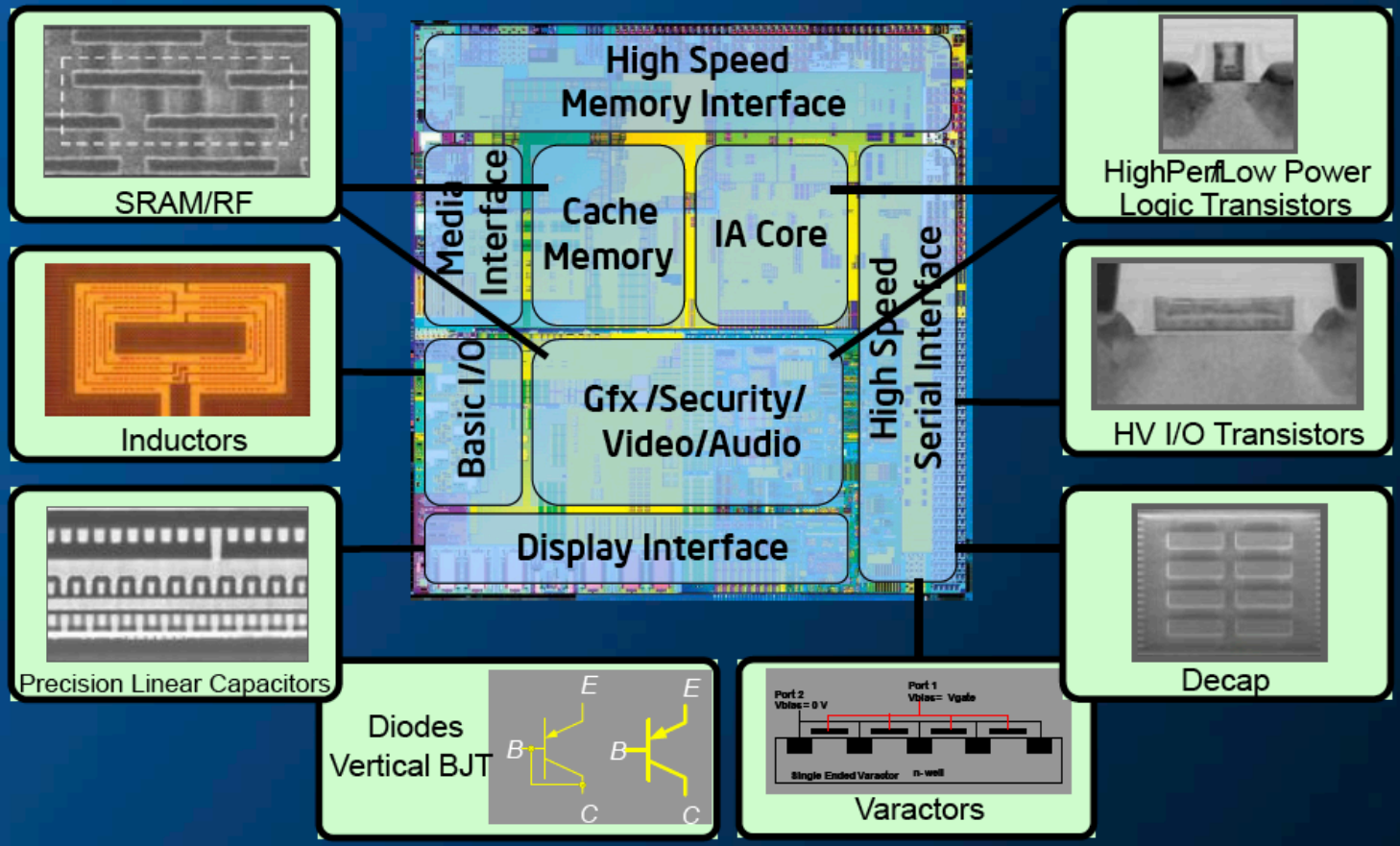
Feb 2017, Intel announced Fab 42 in Arizona will produce microprocessors using 7 nm manufacturing process.

Trend in Cutting Edge Logic Fab

From: https://en.wikichip.org/wiki/technology_node

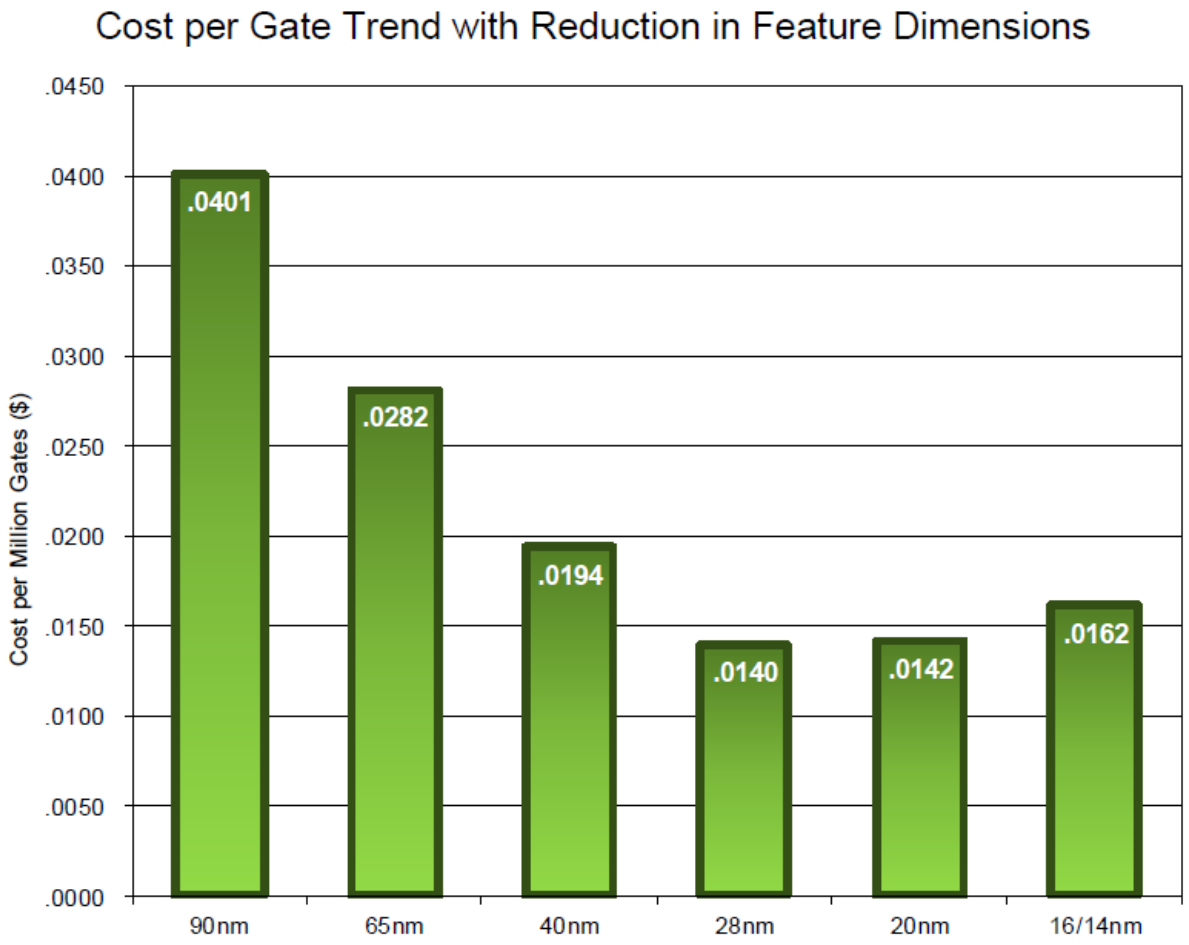
Number of Foundries with a Cutting Edge Logic Fab										
SilTerra X-FAB Dongbu HiTek ADI Atmel Rohm Sanyo Mitsubishi ON Hitachi Cypress Sony Infineon Sharp Freescale Renesas (NEC) SMIC Toshiba Fujitsu TI Panasonic UMC STMicroelectronics IBM AMD Samsung TSMC Intel	ADI Atmel Rohm Sanyo Mitsubishi ON Hitachi Cypress Sony Infineon Sharp Freescale Renesas (NEC) SMIC Toshiba Fujitsu TI Panasonic UMC STMicroelectronics IBM AMD Samsung TSMC Intel	Cypress Sony Infineon Sharp Freescale Renesas (NEC) SMIC Toshiba Fujitsu TI Panasonic UMC STMicroelectronics IBM AMD Samsung TSMC Intel	Renesas (NEC) SMIC Toshiba Fujitsu TI Panasonic UMC STMicroelectronics IBM GlobalFoundries Samsung TSMC Intel	Renesas (NEC) SMIC Toshiba Fujitsu TI Panasonic UMC STMicroelectronics IBM GlobalFoundries Samsung TSMC Intel	Panasonic UMC STMicroelectronics IBM GlobalFoundries Samsung TSMC Intel	IBM GlobalFoundries Samsung TSMC Intel	GlobalFoundries Samsung TSMC Intel	Samsung TSMC Intel	GlobalFoundries Samsung TSMC Intel	Future
180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm

System-on-Chip Building Blocks



SoC products require a broader range of device types than mainstream CPU products

A good reason why deeper scaling might not happen



[Jones]

Maybe Moore's law as we know it may end

… yet there are plenty of interesting challenges and huge opportunities!!

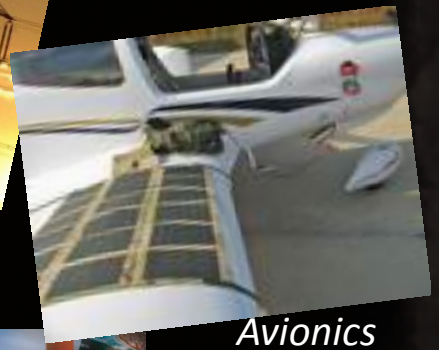
THE IT PLATFORM OF THE NEXT DECADE

TRILLIONS OF CONNECTED DEVICES

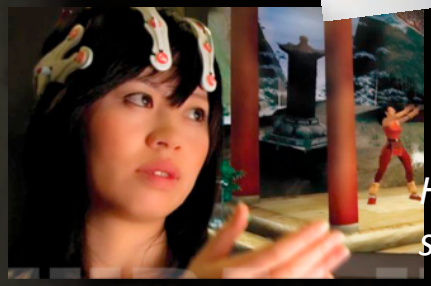
[J. Rabaey, ASPDAC'08]

It's All About Energy

Smart grid



Avionics



Human-centric systems

Compute Cloud

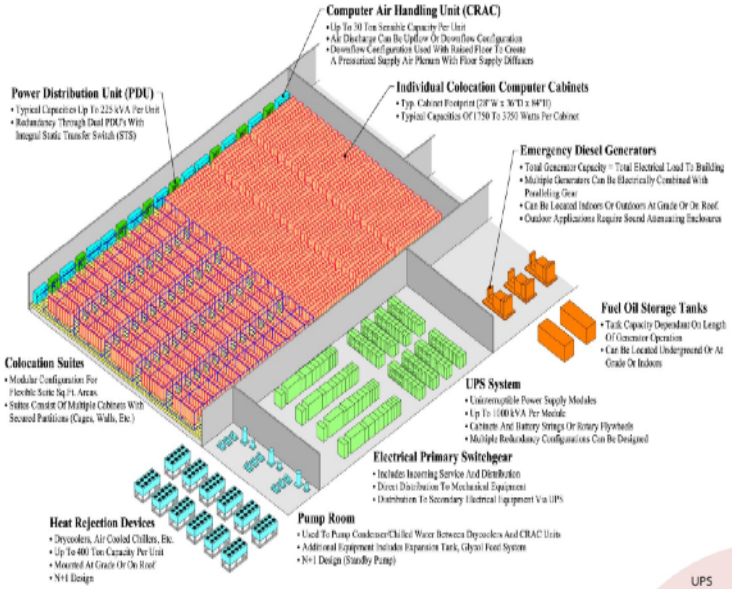
Sensory Swarm

Mobiles

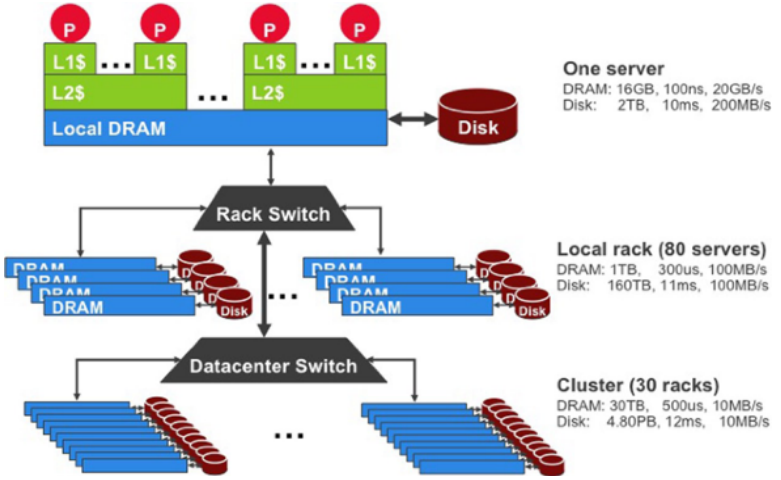
Energy among the most compelling concerns of distributed IT platform and its applications Intelligent energy management at ALL LEVELS AND SCALES offers tremendous opportunity.

DATACENTER ENERGY EFFICIENCY

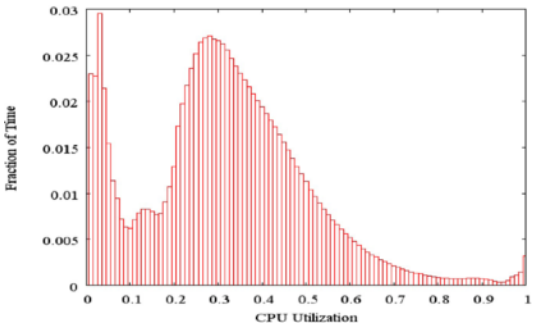
$$\text{Efficiency} = \frac{\text{Computation}}{\text{Total Energy}} = \left(\frac{1}{\text{PUE}}\right) \times \left(\frac{1}{\text{SPUE}}\right) \times \left(\frac{\text{Computation}}{\text{Total Energy to Electronic Components}}\right)$$

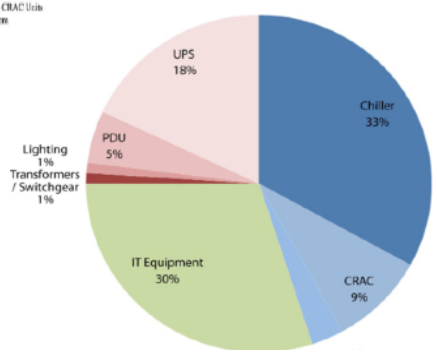


Dyer, ITHERM 2006

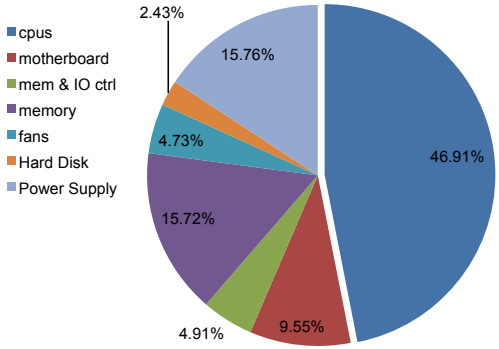


Barroso & Hölzle, 2009





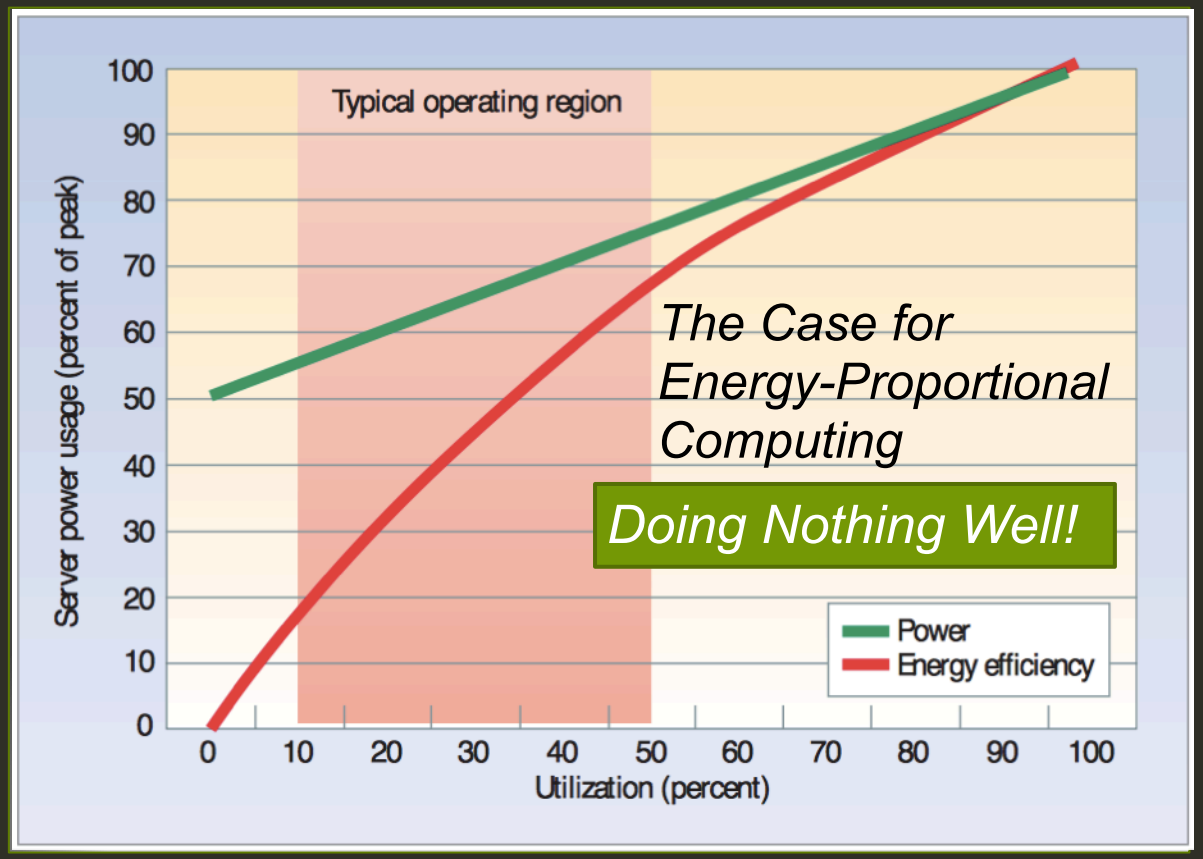
Datacenter energy overhead, ASHRAE



Data and Compute Centers

"The IT workhorses"

[Barroso, Holzle, 2007]



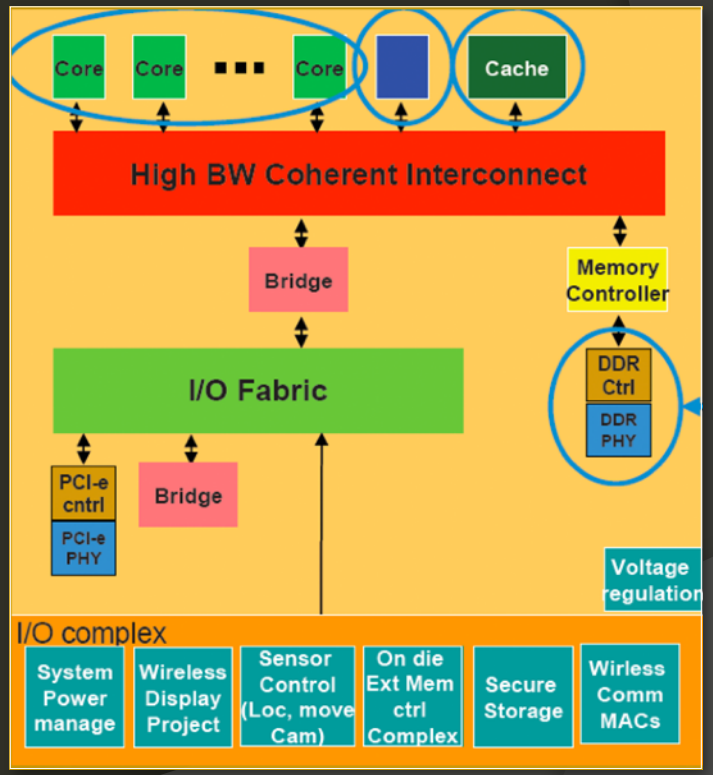
Major Opportunity is in Power Management

Requires Top-Down System Level Solution

Mobiles

"The home of the user interface"

- Most "tricks" already in use! (multi-core, heterogeneity, accelerators, SoC, …)
- Opportunity: system and application considerations
  - *Always-connected*
  - Perceptual processing

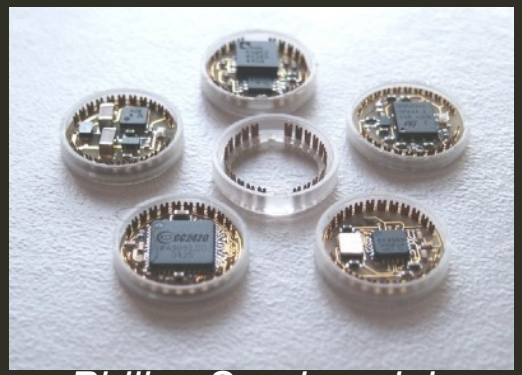


Mobile μProc Anno 2015

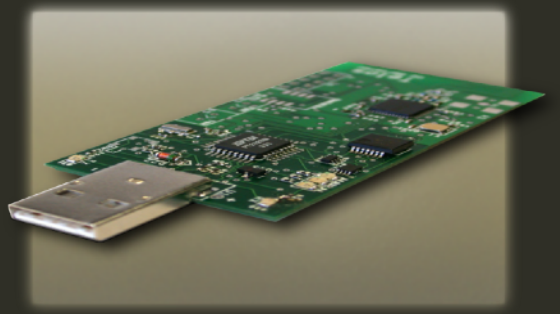
[Courtesy A. Peleg, Intel]

The Sensory Swarm

"Adding senses to the Internet"

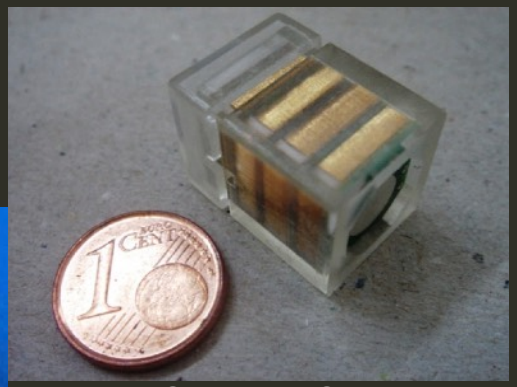


Philips Sand module

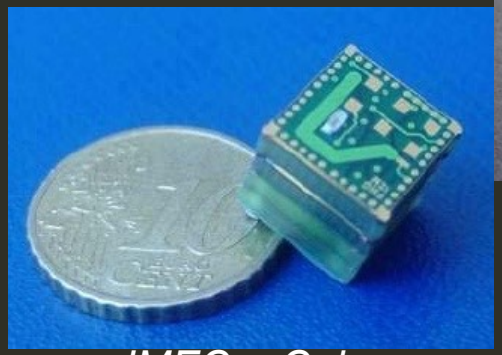


Telos Mote

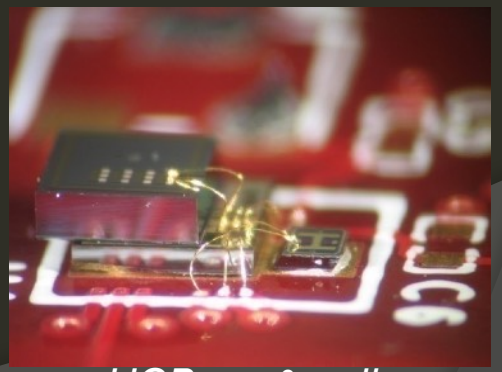
The driver for Ultra-Low Energy design for past decade



UCB PicoCube



IMEC e-Cube



UCB mm^3 radio

[Ref: Ambient Intelligence, W. Weber Ed., 2005]

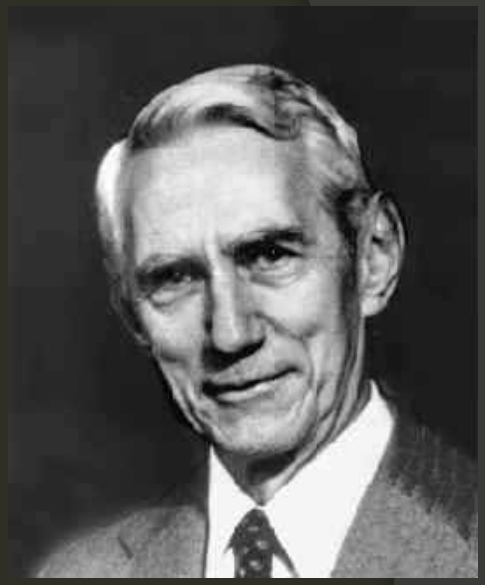
Energy Limits in Digital

John Von Neumann

Shannon-Von Neumann-Landauer Bound:

Minimum energy/ operation = kTln(2)

*= **4.10^{-21}J/bit** at room temperature*



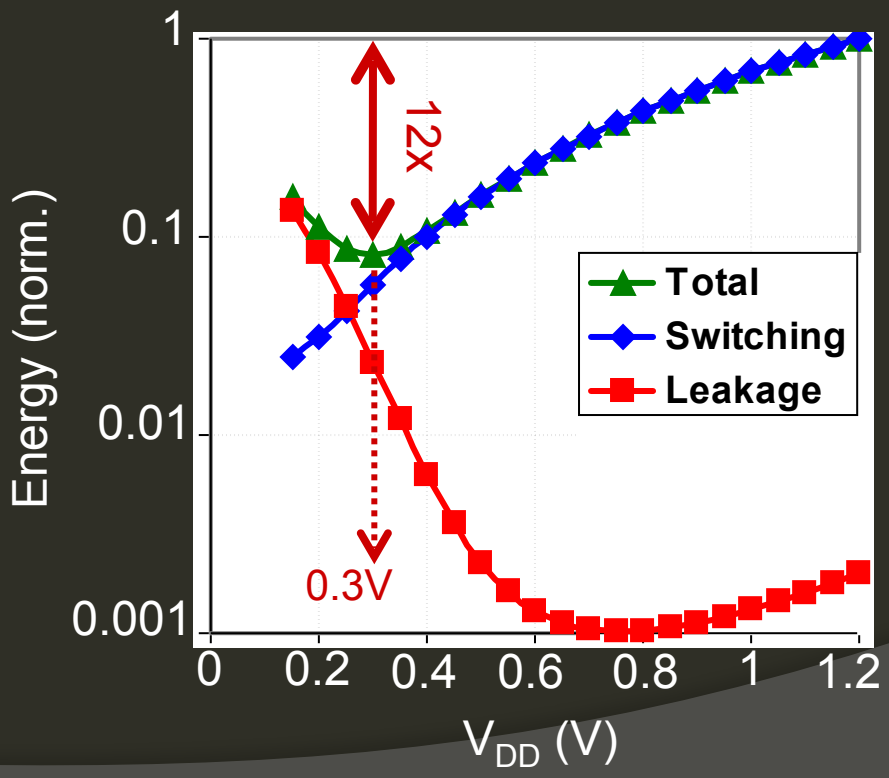
Claude Shannon

More than 4 orders of magnitude below current practice (65 nm at 1V)

Lowering Supply Voltage Only Option

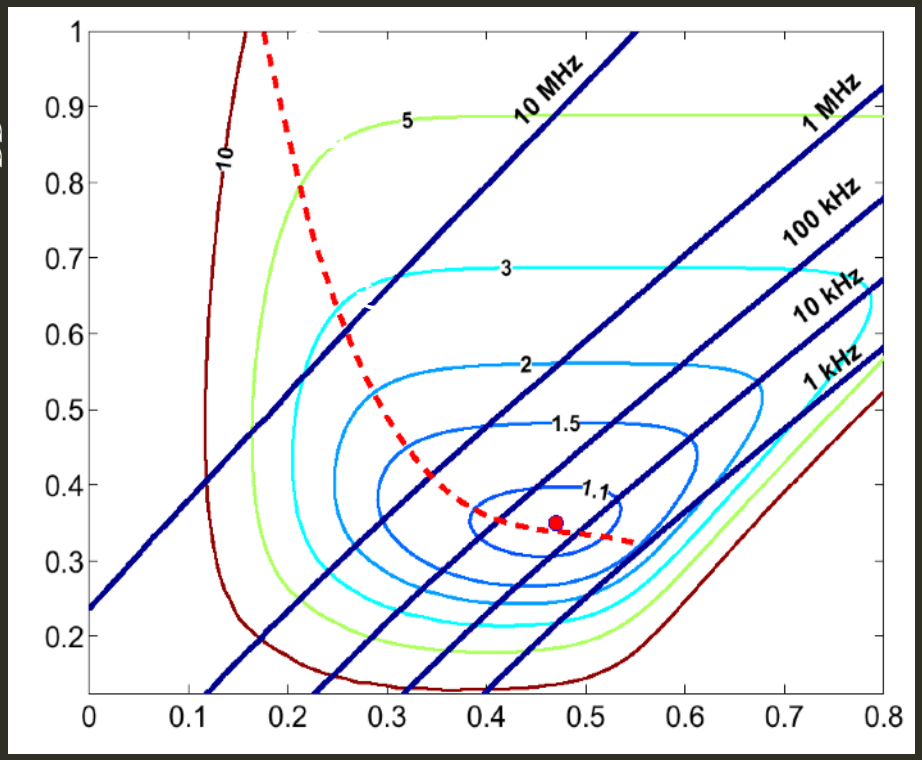
(recoup performance through parallelism)

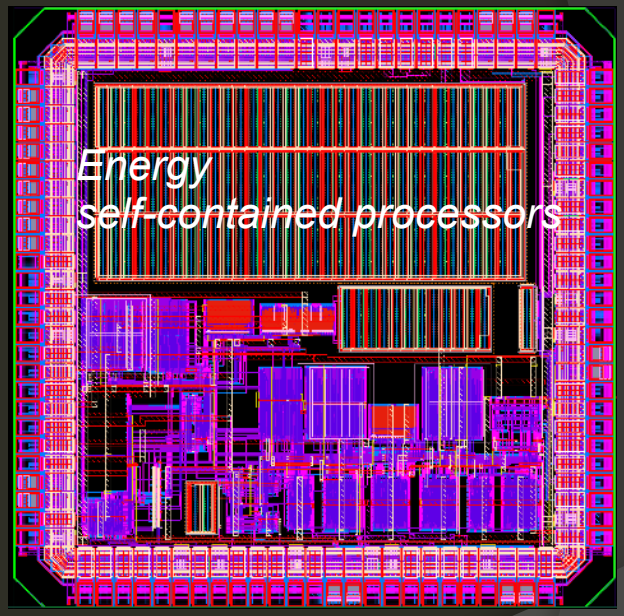
BUT: CMOS Has Minimum Energy Point Set by Leakage



Sub-Threshold Operation Leads to Minimum Energy/Operation

Energy-Aware FFT Processor
[Chang, Chandrakasan, 2004]



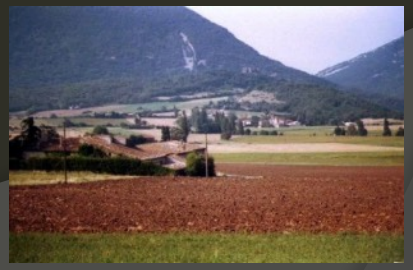


Subliminal μprocessor for retinal implants
3 pJ/inst @ 350 mV
[Blaauw, VLSI'07]

The Age of *CyberPhysical Systems*

Looking Beyond the Devices

Complex collections of sensors, controllers, compute and storage nodes, and actuators that work together to improve our daily lives



Final Exam and Project

- **Final project demo/interview**
  - Next Friday afternoon (make sure you signed up for a slot).
  - Around 15 minutes per group
  - Be prepared to show off your accomplishments and answer questions about your design and process
  - Written report due following week Wed - guidelines to be posted soon.
- **Final exam review session during RRR week**
- **Exam held in scheduled final exam slot**: Friday May 11, 11:30AM-2:30PM, 306 Soda?
  - "Comprehensive" Final Exam
    - We will post a list of semester long important exam topics.

The End.

- Special thanks to our GSIs: Arya and Taehwan
- Good luck on the final
- Thanks for a great semester!