EECS 151/251A Discussion 4

03/02/2018

Announcements

- I'll be in New Zealand next week for a wedding
  - Taehwan will take next week's discussion
  - FPGA labs will be released and will be "due" the following week
  - This is the last time I swear
- Midterm 1 results posted
- Homework 4 will be graded by me on the plane
- Homework 6 coming Real Soon Now

Design Methodology - lec 2 slide 8

- Handwavey concept
- How do we engineer digital systems?
  - Any system?
- Many degrees of freedom. A hard optimisation problem!
- When you’re given a complex thing to build, how do you make the problem tractable?
  - Top-down means:
- What about when the real world details affect what you can abstract? (Think: the electronics)
  - Bottom-up means:

For circuit topics in lectures 9 - 12,

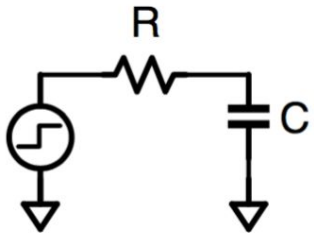
read the recommended not required book [1]

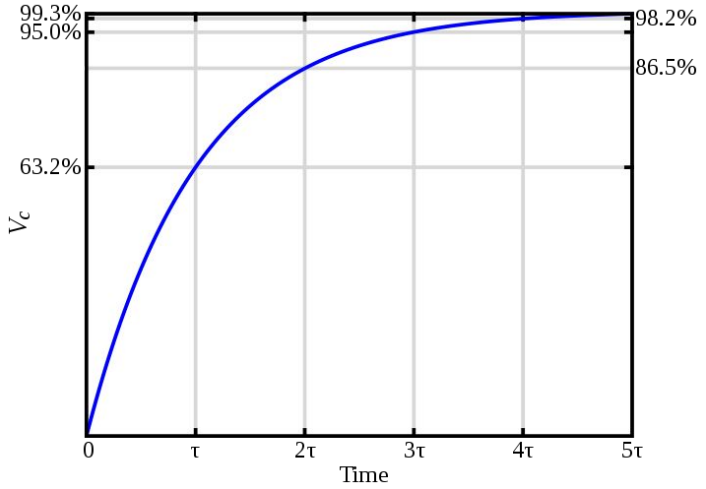
Further reading: [1], ch 5.1 - 5.5

Short-circuit current

Recall the definition of the response of an RC circuit driven by an ideal voltage pulse as below:

$$V_{out}(t) = V_{in}(1 - e^{-\frac{t}{RC}})$$





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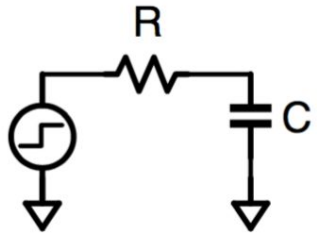


a) How much time (in terms of RC) will it take for V_{out} to rise to 50% of V_{in}? (solve for t)

$$V_{in}/2 = V_{in}(1 - e^{-\frac{t}{RC}}) \Rightarrow 1/2 = 1 - e^{-\frac{t}{RC}} \Rightarrow e^{-\frac{t}{RC}} = 1/2 \Rightarrow -\frac{t}{RC} = ln(1/2) \Rightarrow t = ln(2)RC$$

$$t_{50} = 0.69RC$$

b) How much time will it take for V_{out} to rise to 10% of V_{in}?

$$0.1 \cdot V_{in} = V_{in}(1 - e^{-\frac{t}{RC}}) \Rightarrow -\frac{t}{RC} = ln(0.9)$$

$$t_{10} = 0.105RC$$

c) How much time will it take for V_{out} to rise to 90% of V_{in}?

$$0.9 \cdot V_{in} = V_{in}(1 - e^{-\frac{t}{RC}}) \Rightarrow -\frac{t}{RC} = ln(0.1)$$

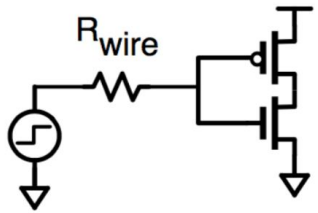
$$t_{10} = 2.3RC$$

d) What is the rise time (10 to 90%)?

$$t_r = t_{90} - t_{10} = 2.2RC$$

For the inverter shown below, assume that the transistors have $R_{on} = 1k\Omega$, $V_{TN} = |V_{TP}| = 0.4$, $C_{in} = 10fF$, $R_{wire} = 1k\Omega$ and $Vdd = 1V$. Use the switch model of the inverter.

e) For a 1V input step, for how long are both transistors on at the same time?



From 0 to 0.4V, the PMOS is on but the NMOS is off, from 0.4V to 0.6V both are on, and from 0.6V to 1V the NMOS is on but the PMOS is off. So we need to find t_{40} and t_{60}.

$$0.6 \cdot V_{in} = V_{in}(1 - e^{-\frac{t}{RC}}) \Rightarrow -\frac{t}{RC} = ln(0.4) \Rightarrow t_{60} = 0.92RC$$

$$0.4 \cdot V_{in} = V_{in}(1 - e^{-\frac{t}{RC}}) \Rightarrow -\frac{t}{RC} = ln(0.6) \Rightarrow t_{40} = 0.51RC$$

$$t_{on} = t_{60} - t_{40} = 0.41RC = 0.41 * 1000 * 10f = 4.1ps$$

f) While both transistors are on, what is the short-circuit power dissipated by the inverter?

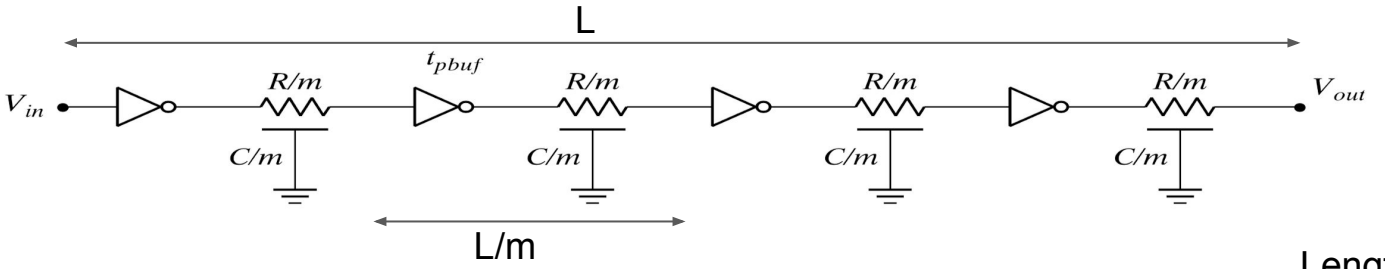
$$P_{sc} = I \cdot V = V^2/R = 1^2/2k = 0.5mW$$

g) Given your answer to part e), what is the total energy dissipated due to the short circuit power you computed in part f)?

$$E = P \cdot t = 0.5mW \cdot 4.1ps = 2.05fJ$$

Further reading: [1], pp 466-467

Wires & Repeaters - lec 12 slide 40



Width of NMOS device

Length of wire

$$t_p = 0.69m\left(\frac{R_N}{W}(W\gamma C_{in} + \frac{cL}{m} + WC_{in}) + \frac{rL}{m}(WC_{in} + 0.5\frac{cL}{m})\right)$$

On-resistance of minimum-sized repeater

Capacitance of wire per unit length

$$m_{opt} = L\sqrt{\frac{rc}{2R_N C_{in}(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

Resistance of wire per unit length

Input capacitance of minimum-sized repeater

$$W_{opt} = \sqrt{\frac{R_N c}{rC_{in}}}$$

Factor of 0.38 in book (from distributed delay) not here)

segments (# repeaters)

Wires & Repeaters - lec 12 slide 40

Book formula uses “drive resistance” R_d and “drive capacitance” C_d instead of R_N and C_{in} respectively). The difference is a factor W:

$R_d = R_N / W$

$C_d = C_{in} \times W$

The book gives a formula for the optimal sizing factor s_{opt}, whereas the lectures give one for W_{opt}, yielding the minimum width directly:

$W_{opt} = s_{opt} \times W_{min}$

Little r, sheet resistance

Conductor is 3D, but we only care about Length (L) and Width (W)

Comes from R eqn for 3D conductor:
(t is thickness)

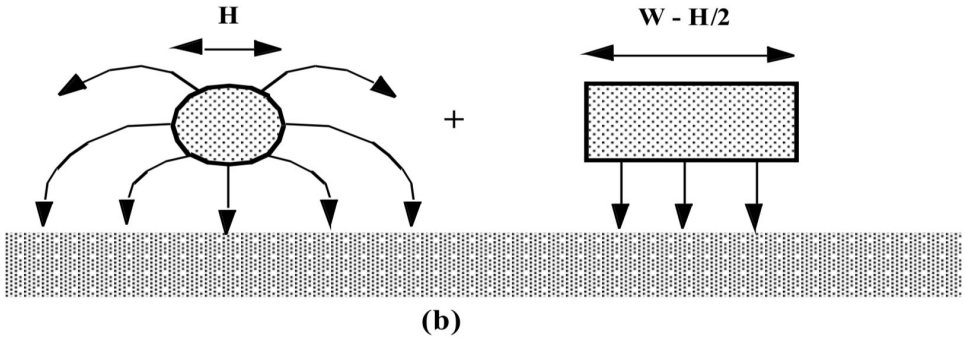
$$R = \frac{\rho}{t}\frac{L}{W} = R_s \frac{L}{W},$$

"Sheet resistance" has units: $\Omega * m^2/m$
Also written Ω/square

Note how you can rearrange the equation to find resistance per length

$$r = R/L = R_s/W \text{ [units: } \Omega/m]$$

Little c, capacitance per unit length



Fringe capacitance, C_{fringe}, does not depend on W, but depends on L

Parallel plate capacitance, C_{pp}, depends on W and L

$$c = C_{pp} * W + C_{fringe} \text{ [units: F/m]}$$

c depends on L

Questions from the floor

That’s you

References

[1] *Digital Integrated Circuits*, Anantha P. Chandrakasan, Borivoje Nikolić, and Jan M. Rabaey

[2] https://en.wikipedia.org/wiki/Sheet_resistance

[3] Past homework problems

[4] More Wikipedia