EECS 151/251A Discussion 7

04/06/2018

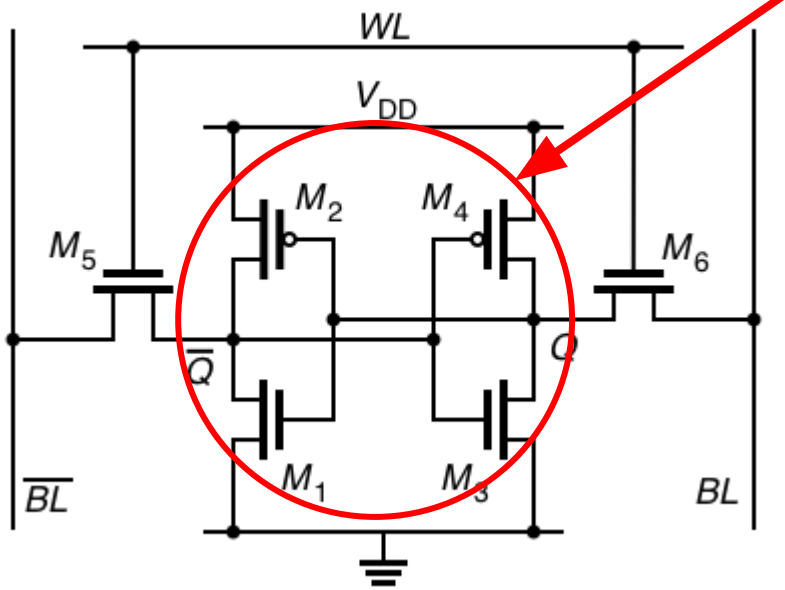
Announcements

- Short discussion today. ~~There will be another next Monday with Taehwan.~~
  - ~~Location/time TBA, slides will be available if you can't make it.~~
- Homework 9 out today

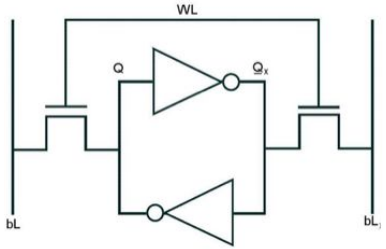
Agenda

- Memories: SRAM
- Your questions

SRAM

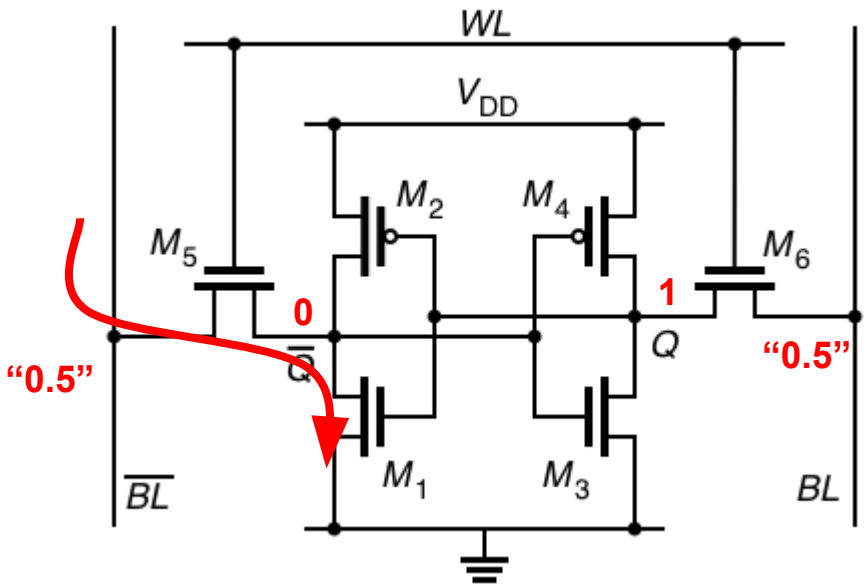


What's this?



Two class CMOS inverters!

How to read?



Assume Q = 1 already.

Pre-charge BL/~BL to $V_{DD}/2$.

Activate WL.

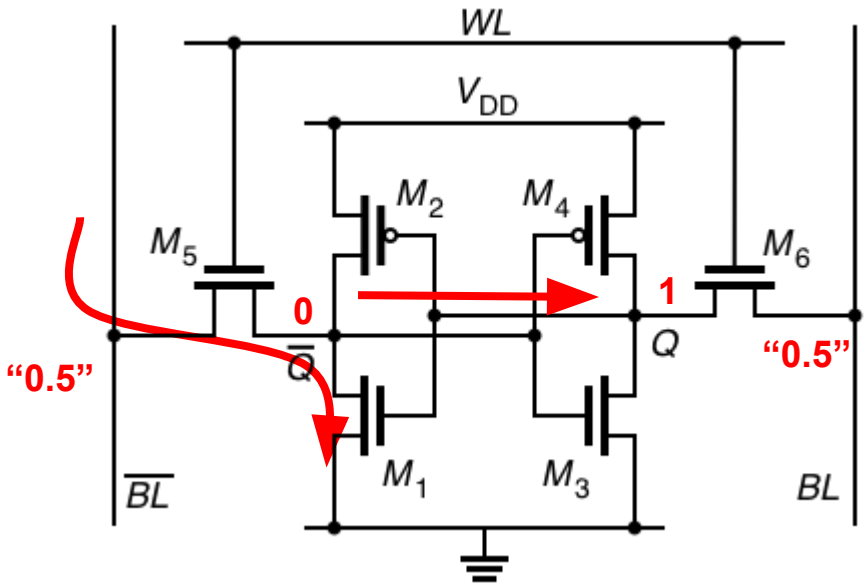
M5 and M6 are on. Don't want Q to change much. Want ~Q pulling ~BL low.

Process is slow. Q connected to BL changes state (we hope slowly).

Sense amplifier speeds up read by detecting BL/~BL shift.

Must size transistors appropriately.

How to size for read?



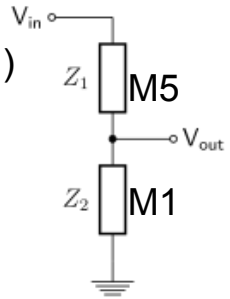
Consider ~Q. Bit line capacitance is high. Initially remains at its precharge value.

Want M1, M5 to be a small as possible → they are slow.

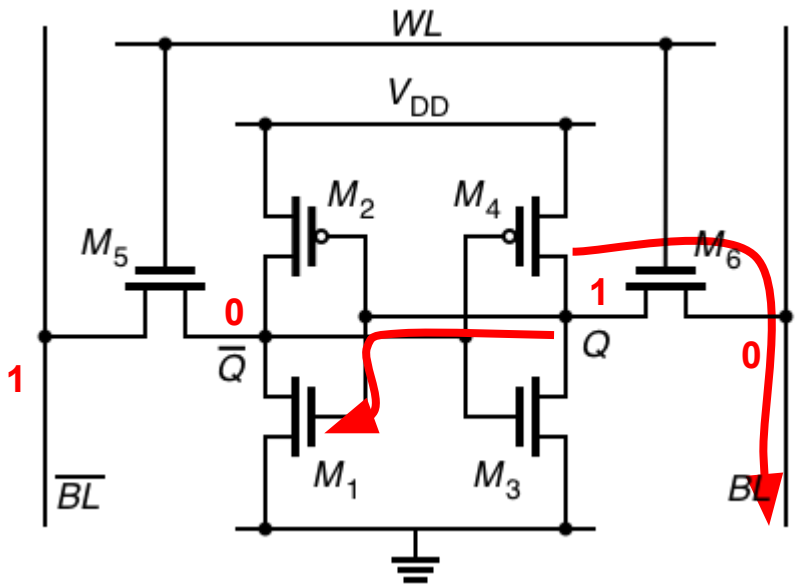
But we need to keep ~Q low enough that M3/M4 stay off!

So the resistance of M5 must be **greater** than M1 to keep this from happening.

(Think of a voltage divider.)



How to write?



Assume Q = 1 already.

Set BL = 0, ~BL = 1.

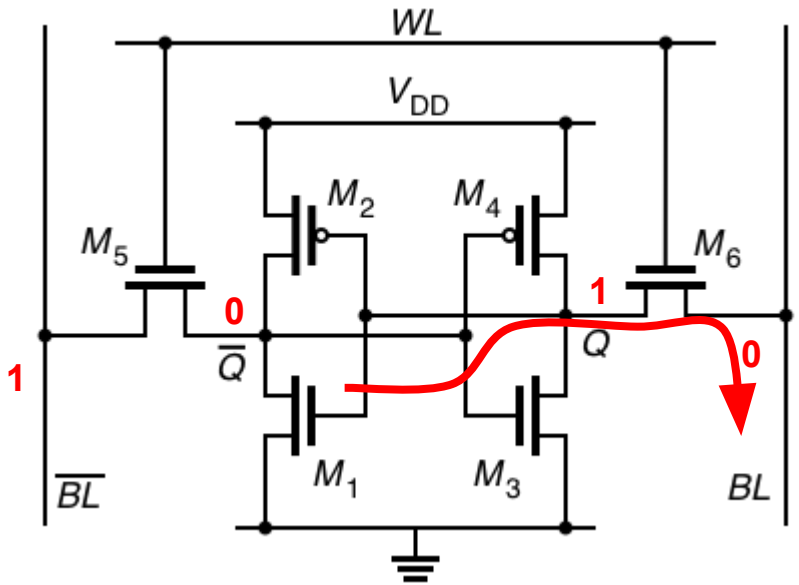
Activate WL.

M6 turns on, draining Q to ground.

M1 starts turning off, raising ~Q.
M3 starts turning on, reducing Q.
Inverters shift, new stable state.

M5 also turns on, connecting ~Q to ~BL. **

How to size for write?



But for the read operation, we sized M5 and M1 such that ~Q *can't* turn M3/M4 on in this situation!

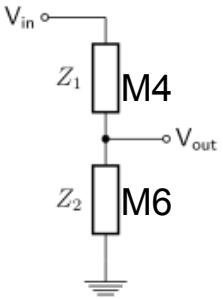
~Q can't be written that way.

Write has to occur through BL to Q.

Q must be pulled low enough to turn M1 off.

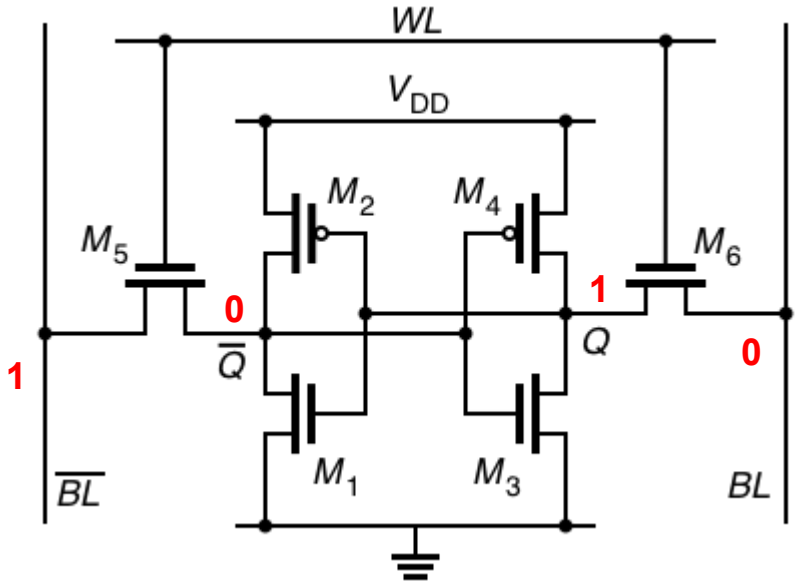
We have another voltage divider in M4 and M6. Want M6 to pull down low enough.

So strength (speed) of M6 > M4, meaning M6 is lower resistance, meaning it is faster.



How to size for write?

It helps that M4 is PMOS, so for similar sizing M6 will be stronger due to its resistivity.



So for writes, M6 stronger than M4. For reads, M1 stronger than M5.

But we've only considered one side of the system. For symmetry (starting with Q = 0), these constraints apply to both sides.

Overall strengths (speeds):
M3 > M6 > M4
M1 > M5 > M2

References

- https://www.embedded-vision.com
- Digital Integrated Circuits, A Design Perspective, 2E, Rabaey et. al.
  - pp 657 - 664
- Digital Design and Computer Architecture, David M. Harris & Sarah L. Harris
- Discussions from EECS151/251A Fall 2017, George Alexandrov
- Homeworks from EECS151/251A Fall 2016, Spring 2017, Fall 2017
- Wikipedia