EECS 151/251A
Final Review: Important Topics

May 1st, 2018

- Introductory Material
  - Concept of Hierarchy in designs and example hierarchies
  - Concept of cost/performance/power tradeoffs and simple examples
  - Chip-level design alternatives and pros and cons of each
  - Economics of FPGAs versus ASICs (NRE versus recurring costs)
- Combinational Logic Basics
  - Function of primitive logic gates
  - Derivation of truth tables from simple combinational logic circuits
  - Derivation of gate circuits from logic equations
  - Derivation of canonical forms
  - Algebraic manipulation for simplification and equivalence checking
  - Signal restoration and its importance in digital circuits
  - Operation and implementation of multiplexors
- Verilog HDL
  - Concept of "behavior" versus "structural" description
  - Module specification and instantiation
  - Basics of combinational logic and sequential circuit specification
  - Continuous assignment versus procedural assignments (both blocking and non-blocking)
  - Use of module parameters and "generate" constructs
- Finite State Machine Design
  - "By hand" design procedure
  - Moore versus Mealy Machines
  - Specification of Finite State Machines
- CMOS circuits

  - Transistor-level circuits for basic logic gates, multiplexors, and flip-flops
  - Implementation of tri-state buffers and their use for bidirectional communication
  - Noise margins
  - Logic sizing - logical effort
  - Delay in wires
  - Repeaters
- Energy and Power
  - Where does energy go in CMOS
  - Energy delay tradeoffs
  - Voltage scaling and parallelism for energy efficiency
  - Power distribtion (IR drop, inductance)
- Timing
  - Relation of clock speed to performance
  - Determination of maximum clock frequency from circuit
  - Hold time violations
  - Origin of logic delay
  - Origin of flip-flop delay
  - Wire delay and mitigation
  - Effects of clock uncertainty
  - Clock distribtion (clock uncertainty: skew, jitter)
- Adders
  - Carry-select adder design principle, cost/performance analysis, optimization
  - Carry look-ahead adder design principle, cost/performance analysis, optimization
  - Bit-serial adders design and operation
- Multiplication
  - Binary multiplication principle
  - Extending multiplication techniques for signed multiplication
  - Combinational (array) multiplier structure and operation
  - Cost-performance analysis of alternative multiplication schemes
  - Bit-serial multiplier structure and operation
  - Carry-save addition technique and application to multiplier design
  - Booth technique
  - Constant multiplication
- Counters
  - Counters in controller design

  - Binary up/down counter design
- Shifters and Cross-bar switch circuits
- Implementation of LFSRs
- Memory
  - Register Files, Caches and FIFOs
  - SRAM organization, arrays, decoders, read-out circuits, cells
  - Multiple ports
  - DRAM cell and read-write operation
  - Cascading memory blocks to increase width/depth/number of ports
  - Operation and implementation of FIFO memories
  - Cache organization
- CPU microarchitecture
  - Implementation of a single-cycle processor from ISA description
  - Processor pipelining: impact on performance, hazard types and resolution
  - Detailed operation of 3-stage MIPS pipeline
- High-Level Design
  - List-processor organization and optimization
  - Register Transfer Language descriptions
  - Pipelining and Retiming
  - Data-level parallelism
  - Loop unfolding/unrolling