EECS 151/251A Homework 1

Due Friday, January 26$^{\text{th}}$, 2018

Problem 1: Computing Systems

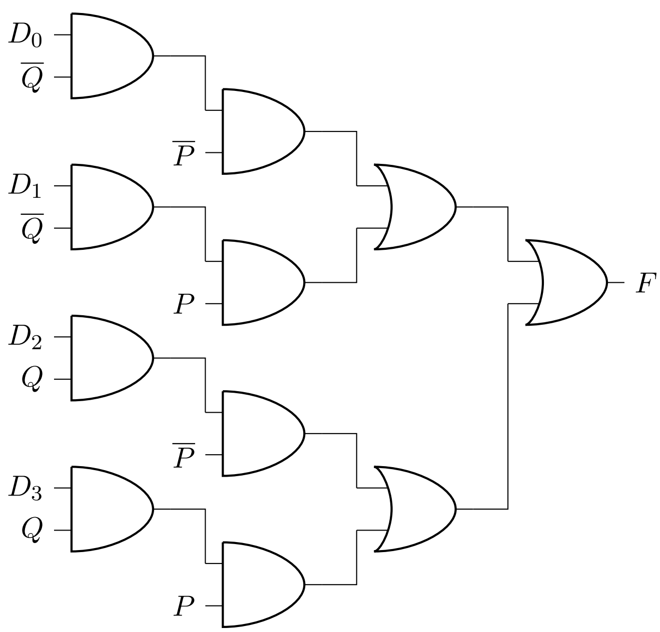
A wide range of computing systems are currently in production. Consider the following devices when answering the questions below: a laptop, a digital watch, a scientific calculator, a supercomputer, and a smartphone.

(a) Sketch a curve showing computational performance of all these systems as a function of their cost. Put performance on the y-axis (arbitrary units), and cost on the x-axis (dollar estimate).

(b) Similarly, show a curve that relates computational performance to system power con- sumption, with performance on the y-axis (arbitrary units), and power consumption on the x-axis (watt estimate). In the case of the smartphone, ignore the power consumption of the radio.

Problem 2: Logic

Consider the circuit below. All inputs (P, Q, D_0, D_1, D_2, and D_3) must be tied to 0 or 1.



(It might help to simplify this circuit, as you would with the kind of powerful diagramming tool I do not have.)

(a) What must D_0, D_1, D_2, D_3 be such that $F = P \oplus Q$?

(b) Can any arbitrary 2 input logic function of signals P and Q be realized using the above architecture? Explain.

Problem 3: Logical Gates

You work for Sldgly, a start-up in San Francisco that uses the sludge found in the Bart transit system to perform logic functions. They call this device a Sludge Gate; every Sludge Gate requires a supply and ground, has input signals X and Y, and produces an output signal Z.

Here is the behavior of the Sludge Gate with a 5 V supply:

- $0 < Z < 5V$
- If X and Y have less than 2 V at the input for 5 microseconds or more, then Z is greater than 4 V
- When either or both of X and Y have more than 3.5 V for at least 5 microseconds, then Z is less than 1 V

The exact voltage at Z is unpredictable and varies from Sludge Gate to Sludge Gate.

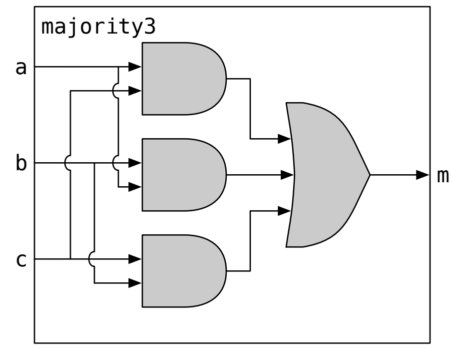
(a) Propose a simple topology using Sludge Gates to invert an input signal, S.

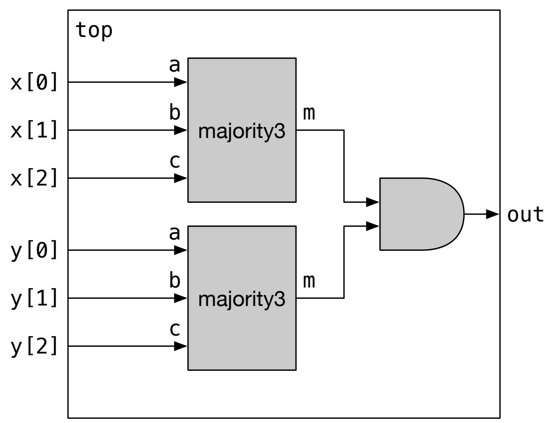
(b) For the inverter in (a) draw a very simple voltage transfer curve, making sure to label key voltages on both axes.

(c) What Boolean function of X and Y does the Sludge Gate implement?

Problem 4: Structural Verilog

Write modules using structural Verilog which implement the circuit drawn below. You will need multiple `module` statements to preserve the hierarchy as drawn.





Problem 5: Behavioral Verilog

For the logic circuit shown below, write the equivalent behavioral Verilog module which takes A and B as inputs, and gives X as output.