EECS 151/251A Homework 11

Due Monday, April 30th, 2018

Problem 1:

(a) Suppose we need to transfer a video signal over a connection with a maximum bandwidth of 10^8 bits/s. Our video frame has 1000×1000 pixels, and a frame rate of 25 frames/s. What is the maximun number of bits per pixel that we can send?

(b) Approximately how much storage (in bytes, B) is needed to store 3 minutes of uncompressed stereo music?

(c) Given a 10/100/1000 Ethernet link operating at a line rate of 1 Gb/s (and assuming the producer is able to supply data at arbitrarily high rates), how much time would a transfer of 100 million bytes of raw data take (no protocol embedded into the Ethernet frames)?

Assume that no inter-frame gap is needed, and "Jumbo" frames are disallowed.

Problem 2:

You are an engineer at AcmeVideo, Inc. Your current display system has the following specifications:

- 30 frames/second
- black & white display (only one component for each pixel)
- 8 bits per pixel
- 600 pixels/line
- 600 lines/frame

The display system uses a frame buffer based on an SDRAM with the following specifications:

- 8-bit data interface
- 4+L cycles per read or write access, where L = burst length (consecutive memory accesses, 1 per cycle)
- Maximum L = 6
- 48 MHz clock frequency

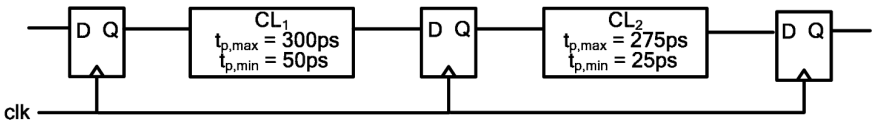
Your marketing department would like to bring out a new product based on your current display system. It will have a display monitor that can be rotated 90 degrees and a mechanical switch to detect when the monitor is rotated. When the monitor is rotated, the display system must rotate the video output by 90 degrees to compensate. Your VP of engineering has decided that the cheapest way to achieve this compensation is to transform the image using the frame-buffer; it will be written to the frame buffer row-by-row, but read out column-by-column.

(a) Using the existing frame buffer and changing the control logic, is it possible to support the rotation operation and maintain the display specifications? Show your work.

(b) Adhering to all other specs, what is the maximum display refresh rate when rotated?

Problem 3: Timing and Clock Distribution

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{clk-q} = 50ps$, $t_{setup} = 25ps$, and $t_{hold} = 25ps$. You can assume that the clock has no jitter.

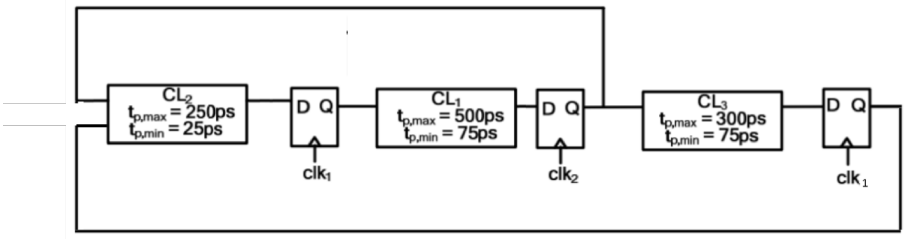


(a) What is the minimum clock cycle time for this pipeline? Are there any minimum delay violations?

(b) Under these same conditions (i.e., 50ps nominal inverter delay, +/-20% delay variation), can this pipeline fail any minimum delay constraints?

Problem 4: Timing

Consider the following logic function. The minimum and maximum delays of the logic modules are annotated on the figure. The flip-flops have the following timing properties: $t_{clk-q} = 50ps$, $t_{setup} = 50ps$, and $t_{hold} = 25ps$. You may assume that the clock has no jitter.



(a) Assuming that there is no skew between clocks, what is the minimum clock cycle time for this pipeline?

(b) Under the conditions established so far, does the circuit meet all hold time requirements? Explain.

(c) Now lets assume that clk_1 and clk_2 can be randomly skewed *relative to each other* by up to +/-60ps. What is the minimum clock cycle time under those conditions? Does this solution cause hold time violations?

(d) **EECS 251A Only.** Consider the circuit given below, in which is clk_1 is replaced by an independent clock clk_3 at the last stage. You may now intentionally choose any skew you would like between clk_1, clk_2 and clk_3. Ignoring hold time violations, what would be the smallest possible cycle time? Please explain how you would skew the different clocks.