EECS 151/251A Homework 11

Due Monday, April 30th, 2018

Problem 1:

(a) Suppose we need to transfer a video signal over a connection with a maximum bandwidth of 10^8 bits/s. Our video frame has 1000×1000 pixels, and a frame rate of 25 frames/s. What is the maximun number of bits per pixel that we can send?

(b) Approximately how much storage (in bytes, B) is needed to store 3 minutes of uncompressed stereo music?

(c) Given a 10/100/1000 Ethernet link operating at a line rate of 1 Gb/s (and assuming the producer is able to supply data at arbitrarily high rates), how much time would a transfer of 100 million bytes of raw data take (no protocol embedded into the Ethernet frames)?

Assume that no inter-frame gap is needed, and "Jumbo" frames are disallowed.

Problem 2:

You are an engineer at AcmeVideo, Inc. Your current display system has the following specifications:

- 30 frames/second
- black & white display (only one component for each pixel)
- 8 bits per pixel
- 600 pixels/line
- 600 lines/frame

The display system uses a frame buffer based on an SDRAM with the following specifications:

- 8-bit data interface
- 4+L cycles per read or write access, where L = burst length (consecutive memory accesses, 1 per cycle)
- Maximum L = 6
- 48 MHz clock frequency

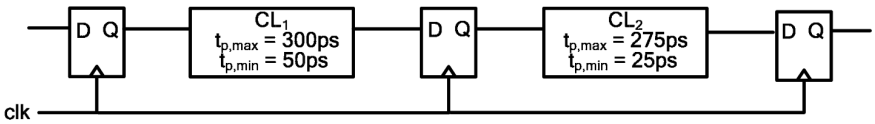
Your marketing department would like to bring out a new product based on your current display system. It will have a display monitor that can be rotated 90 degrees and a mechanical switch to detect when the monitor is rotated. When the monitor is rotated, the display system must rotate the video output by 90 degrees to compensate. Your VP of engineering has decided that the cheapest way to achieve this compensation is to transform the image using the frame-buffer; it will be written to the frame buffer row-by-row, but read out column-by-column.

(a) Using the existing frame buffer and changing the control logic, is it possible to support the rotation operation and maintain the display specifications? Show your work.

(b) Adhering to all other specs, what is the maximum display refresh rate when rotated?

Problem 3: Timing and Clock Distribution

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{clk-q} = 50ps$, $t_{setup} = 25ps$, and $t_{hold} = 25ps$. You can assume that the clock has no jitter.



(a) What is the minimum clock cycle time for this pipeline? Are there any minimum delay violations?

The path with the largest delay is CL_1, therefore to calculate the minimum clock cycle time:

$$t_{clk-q} + t_{p,max,CL_1} + t_{setup} \leq T_{clk} \Rightarrow$$

$$T_{clk} \geq 50ps + 300ps + 25ps \Rightarrow$$

$$\boxed{T_{clk} \geq 375ps}$$

The path with the shortest delay is CL_2, so we need to check it for hold time violations:

$$t_{clk-q} + t_{p,min,CL_2} \geq t_{hold} \Rightarrow$$

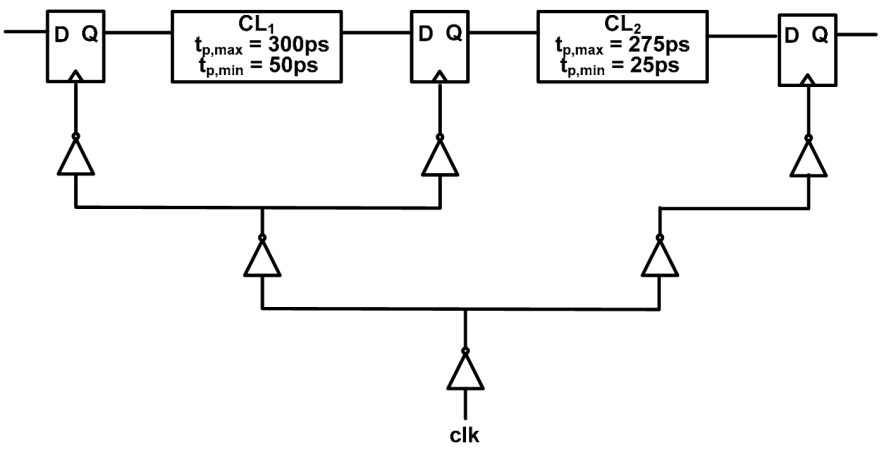
$$50ps + 25ps \geq 25ps$$

$$75ps \geq 25ps$$

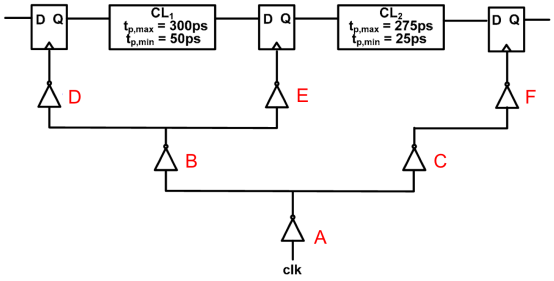
So there are no hold-time violations.

(b) Now we include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 50ps, but that each inverter's delay varies randomly by +/-20%, now what is the minimum clock cycle time?

In the presence of variations, the worst-case for delay is when the clock cycle becomes shorter, since now we have less time to evaluate. Looking at the two paths, we need to determine



what combination of clock skew causes the worst-case. Each inverter can vary by $\pm 10ps$. CL_1 has the max delay, but note that its clocks come from a balanced tree, so it only picks up skew from the last stage (inverters D and E). On the other hand, CL_2 picks up skew from the two last stages (inverters B,E,C,F). In this case, we need to check both cases since it is not immediately clear which one will be critical.



For CL_1, the max skew added is 20ps ($t_{skew,D} = +10ps, t_{skew,E} = -10ps$), so:

$$t_{clk-q} + t_{p,max,CL_1} + t_{setup} \leq T_{clk} - t_{skew,max} \Rightarrow$$

$$50ps + 300ps + 25ps \leq T_{clk} - 20ps \Rightarrow$$

$$T_{clk} \geq 395ps$$

For CL_2, the max skew added is 40ps ($t_{skew,E} = +10ps + 10ps, t_{skew,F} = -10ps - 10ps$), so:

$$t_{clk-q} + t_{p,max,CL_1} + t_{setup} \leq T_{clk} - t_{skew,max} \Rightarrow$$

$$50ps + 275ps + 25ps \leq T_{clk} - 40ps \Rightarrow$$

$$T_{clk} \geq 390ps$$

Therefore the worst-case is stil CL_1, and $\boxed{T_{clk} \geq 395ps}$.

(c) Under these same conditions (i.e., 50ps nominal inverter delay, +/-20% delay variation), can this pipeline fail any minimum delay constraints?

Once again, we need to find what the worst-case for hold-time is. CL_2 has the shortest delay and, like before, has the most skew added, so it is going to be the critical case. For hold-time, the worst-case occurs when the skew makes the capture edge arrive late, therefore allowing for more time for the data to race through. So, the worst-case skew will be again $40ps$, but this time the clock on E arrives early and the clock on F arrives late ($t_{skew,E} = -10ps - 10ps, t_{skew,F} = +10ps + 10ps$).

$$t_{clk-q} + t_{p,min,CL_2} \geq t_{hold} + t_{skew,max} \Rightarrow$$

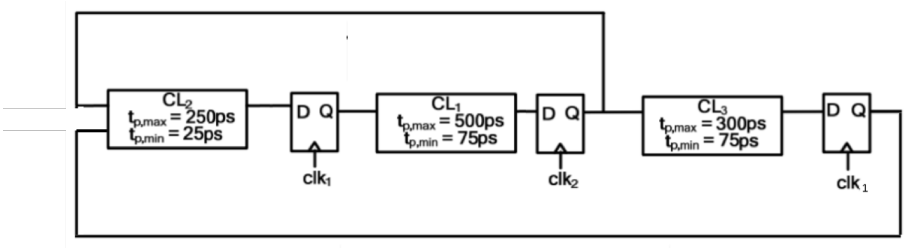
$$50ps + 25ps \geq 25ps + 40ps$$

$$75ps \geq 65ps$$

So there are no hold-time violations.

Problem 4: Timing

Consider the following logic function. The minimum and maximum delays of the logic modules are annotated on the figure. The flip-flops have the following timing properties: $t_{clk-q} = 50ps$, $t_{setup} = 50ps$, and $t_{hold} = 25ps$. You may assume that the clock has no jitter.



(a) Assuming that there is no skew between clocks, what is the minimum clock cycle time for this pipeline?

The longest delay is on path CL_1:

$$t_{clk-q} + t_{p,max,CL_1} + t_{setup} \leq T_{clk} \Rightarrow$$

$$T_{clk} \geq 50ps + 500ps + 50ps \Rightarrow$$

$$\boxed{T_{clk} \geq 600ps}$$

(b) Under the conditions established so far, does the circuit meet all hold time requirements? Explain.

The shortest delay is on path CL_2:

$$t_{clk-q} + t_{p,min,CL_1} \geq t_{hold} \Rightarrow$$

$$50ps + 25ps \geq 25ps$$

$$75ps \geq 25ps$$

So there is no hold-time violation.

(c) Now lets assume that clk_1 and clk_2 can be randomly skewed *relative to each other* by up to +/-60ps. What is the minimum clock cycle time under those conditions? Does this solution cause hold time violations?

The first thing to note is that the skew is given *relative to each other*. This means that the maximum skew that can be added in a cycle is $60ps$ (*not* $120ps$). Since the max delay of path CL_1 is much longer than that of the other paths (i.e. much more than $60ps$), this is going to be the worst-case for delay. The worst-case occurs when the skew shortens the cycle i.e. if we use clk1 as a reference ($t_{skew,clk1} = 0$) then $t_{skew,clk2} = -60ps$ would give us the worst-case.

$$t_{clk-q} + t_{p,max,CL_1} + t_{setup} \leq T_{clk} - t_{skew,max} \Rightarrow$$

$$T_{clk} \geq 50ps + 500ps + 50ps + 60ps \Rightarrow$$

$$\boxed{T_{clk} \geq 660ps}$$

For hold time:

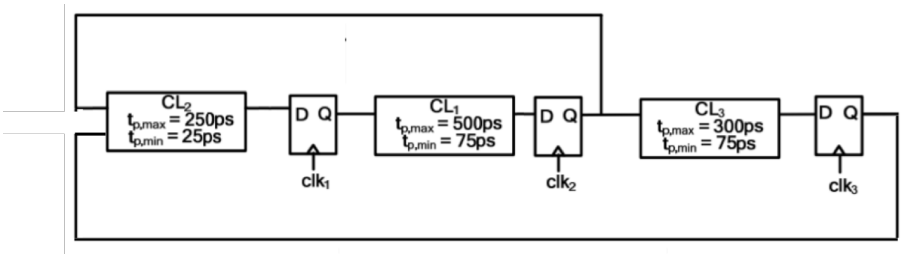
$$t_{clk-q} + t_{p,min,CL_1} \geq t_{hold} + t_{skew,max} \Rightarrow$$

$$50ps + 25ps \geq 25ps + 60ps$$

$$75ps \geq 85ps$$

So there is a hold-time violation.

(d) **EECS 251A Only.** Consider the circuit given below, in which is clk_1 is replaced by an independent clock clk_3 at the last stage. You may now intentionally choose any skew you would like between clk_1, clk_2 and clk_3. Ignoring hold time violations, what would be the smallest possible cycle time? Please explain how you would skew the different clocks.



Again, we will use $clk1$ as a reference and we will define $t_{skew1} = t_{clk2} - t_{clk1}$ and $t_{skew2} = t_{clk3} - t_{clk1}$. Note that both t_{skew1} and t_{skew2} could be positive or negative.

The total delay in the circuit is $t_{p,tot} = t_{p,max,CL_2} + t_{p,max,CL_1} + t_{p,max,CL_3} = 250p + 500ps + 300ps = 1050ps$. If this was a perfectly balanced pipeline (i.e. all logic blocks have equal delay) then each block would have a delay of $t_{p,tot}/3 = 350ps$ and the minimum clock cycle would be $t_{clk-q} + t_{p,tot}/3 + t_{setup} = 450ps$. Theoretically, this circuit cannot do any better than that, so this is our first optimization target.

Looking at the slowest path (CL_1) we have:

$$t_{clk-q} + t_{p,max,CL_1} + t_{setup} \leq T_{clk} + t_{skew1} \Rightarrow T_{clk} + t_{skew1} \geq 600ps \quad (1)$$

In order to get $T_{clk} = 450ps$ we need $t_{skew1} = 150ps$. Then for path CL_2 ($clk2 \rightarrow clk1$) we have:

$$t_{skew1} + t_{clk-q} + t_{p,max,CL_2} + t_{setup} \leq T_{clk} \Rightarrow T_{clk} - t_{skew1} \geq 350ps \quad (2)$$

So selecting $t_{skew1} = 150ps$ makes path CL_2 ($clk2 \rightarrow clk1$) critical (note that path CL_3 could also be critical, but that could be adjusted through t_{skew2}). Therefore, *it is not possible to achieve the theoretical minimum delay in this circuit.*

To solve this problem we will solve the system of inequalities (1) and (2), in order to find the amount of skew that can satisfy both inequalities. This gives us $t_{skew1} \leq 125ps$. Therefore, we select $\boxed{t_{skew1} = 125ps}$ and then $T_{clk,min} = 475ps$ from CL_1 and CL_2, and we still need to check CL_3.

Looking at CL_3:

$$t_{clk-q} + t_{p,max,CL_3} + t_{setup} \leq T_{clk} + (t_{skew2} - t_{skew1}) \Rightarrow T_{clk} + t_{skew2} \geq 525ps \tag{3}$$

From (3) we get $\boxed{t_{skew2} = 50ps}$ in order to maintain a $475ps$ clock cycle.

The last path that we need to check is CL_2 ($clk3 \rightarrow clk1$):

$$t_{skew2} + t_{clk-q} + t_{p,max,CL_2} + t_{setup} \leq T_{clk} \Rightarrow T_{clk} \geq 400ps \tag{4}$$

So this path is still not critical. Therefore the minimum cycle is $\boxed{T_{clk} = 475ps}$ and it is achieved using $\boxed{t_{skew1} = 125ps}$ and $\boxed{t_{skew2} = 50ps}$.