# EECS 151/251A Homework 3

Due Sunday, February 11$^{\text{th}}$, 2018

## Problem 1: Boolean Identities

(a) De Morgan's laws are useful in simplifying some boolean expressions; they are given as follows:

$$\overline{A \cdot B} \equiv \overline{A} + \overline{B}$$
$$\overline{A + B} \equiv \overline{A} \cdot \overline{B}$$

Prove these laws are true by equating truth tables derived from either side of the law.

(b) Use De Morgan's laws to describe how to construct:

  (a) an AND gate from a NOR gate and inverters
  (b) an OR gate from a NAND gate and inverters

(Hint: Invert both sides of each De Morgan law).

(c) Construct a NOR gate in terms of NAND gates and inverters, and construct a NAND gate in terms of NOR gates and inverters

(d) Manipulate the XOR boolean expression $XOR(A, B) = (A + B) \cdot (\overline{A} + \overline{B})$ to construct it using only NAND gates and inverters.

## Problem 2: Logic Simplification

Take this truth table consisting of 4 input variables and 1 output.

| A | B | C | D | Out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | x |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

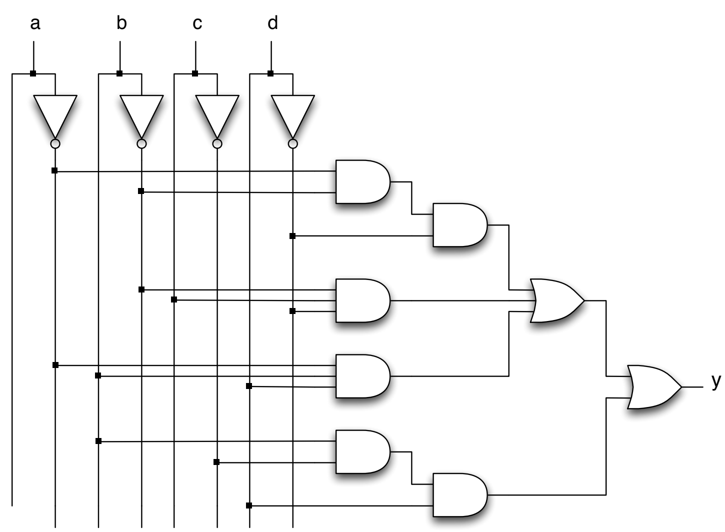
where 'x' means don't care.

(a) Write a sum of products boolean function directly from the truth table

(b) Use a 4 variable Karnaugh Map to derive a simplified boolean function from this truth table.

## Problem 3: Representations of Combinational Logic

For the following circuit,




1. Write a Boolean equation that represents the function of the circuit.
2. Draw and fill in the truth table.

3. Write the sum-of-products canonical form for this function.

## Problem 4: Combinational Logic

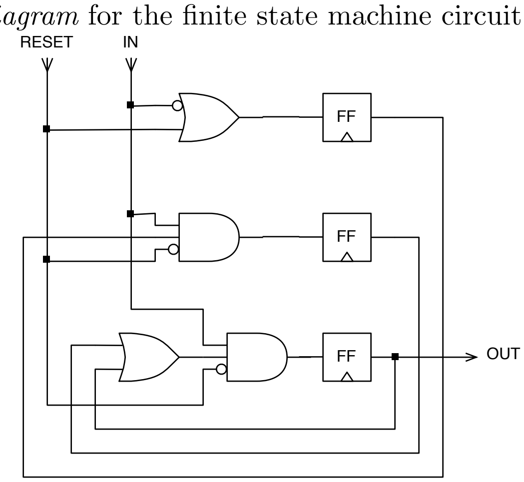
Consider the design of a combinational logic circuit that compares two 9-bit integers for equivalence (an "equal comparator"). The circuit takes 2 9-bit integers A, and B, and outputs 1 on **z** iff A≡B.

Your solution can include any combination of: inverters, 2-input AND gates, 2-input OR gates, 2 to 1 multiplexors, and 2-input exclusive-OR gates. Your goal is to minimize the delay through the circuit. You can assume that the delay through each of these components is the same.

In the space below neatly draw the circuit diagram for your equal comparator. Label all inputs and outputs.

## Problem 5: Finite State Machine

Draw the *state transition diagram* for the finite state machine circuit shown below.




**Optional:** What is the maximum *clock frequency* for this circuit? Assume IN comes from the OUT of an identical copy of this circuit, all logic gates have a delay of 1ns and the flip-flop setup time and clock-to-q delay are both 0.5ns.