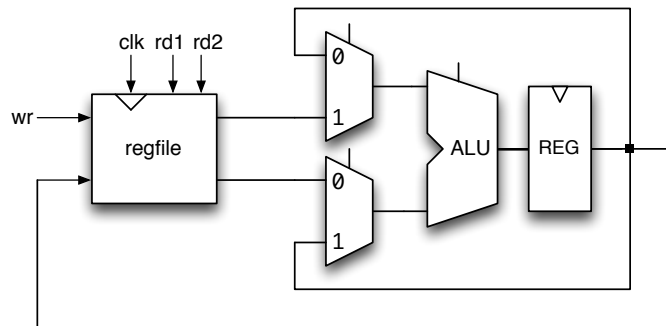


EECS 151/251A Homework 5

Due Monday, March 5th, 2018

Problem 1: Timing

The data-path shown below is used in a simple processor.

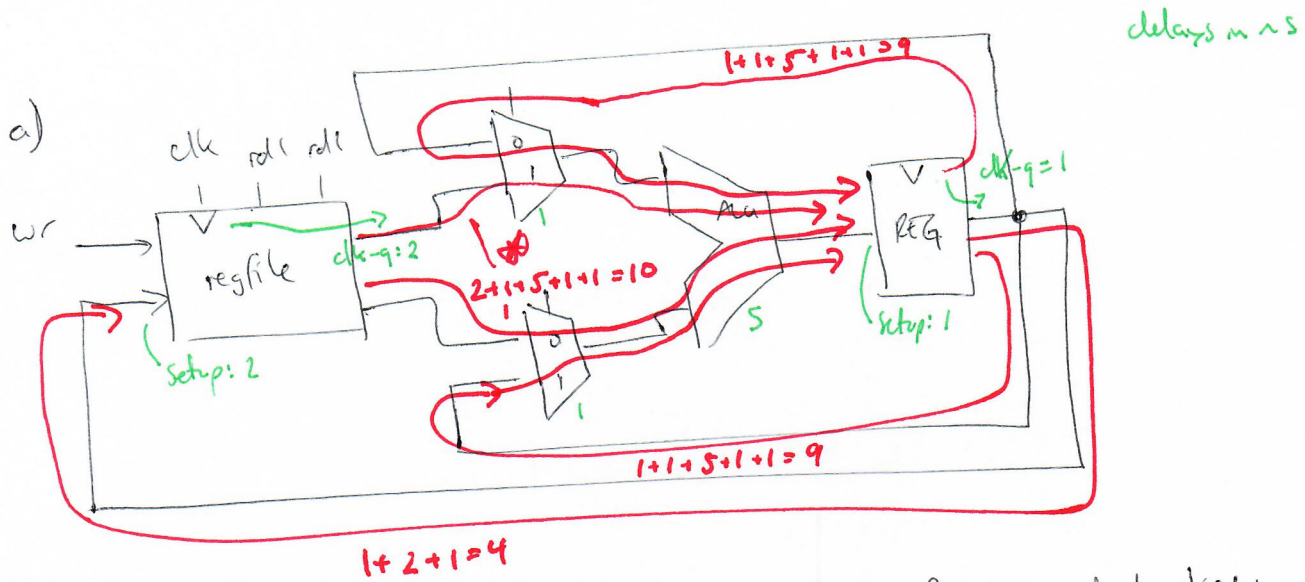


The elements used in the design have the following timing characteristics. The worst case clock skew is 1ns. For this problem you can ignore the delay in the controller.

	setup-time	clock-to-q	CL delay
regfile	2ns	2ns	-
register	1ns	1ns	-
mux	-	-	1ns
ALU	-	-	5ns

1. What is the minimum clock period for this design? Show your work.
2. Can you improve the clock frequency by rearranging the elements in the data-path (and adding more hardware if needed), but keeping the same function? If so, what is the new minimum clock period? Show your design.

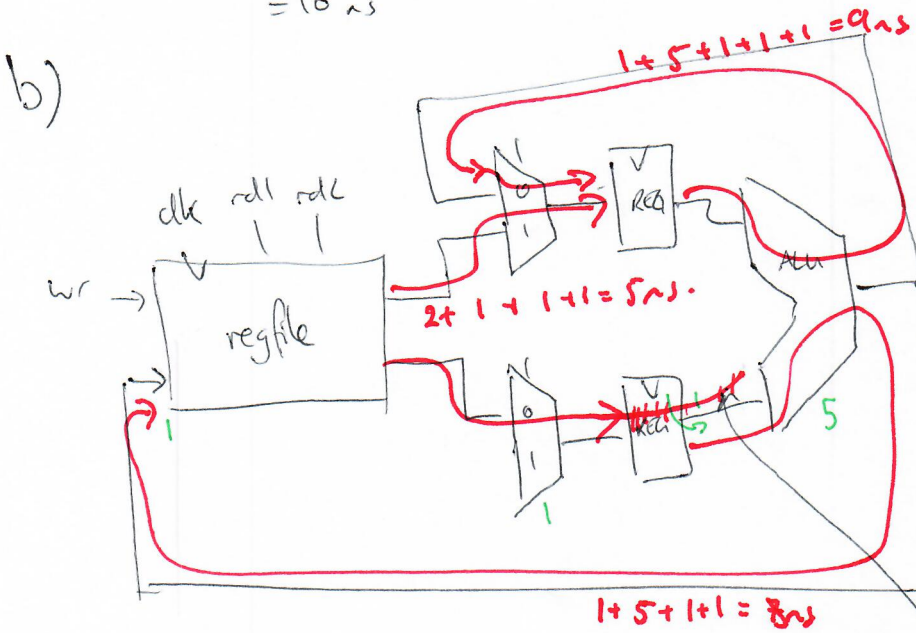
Homework 5 Problem 1 Solutions.



For every path, add 1ns delay to account for the clock skew - clock at receiver may be an extra 1ns away when your data arrives.

Minimum clock period is 10ns from path (10).

$$\begin{aligned}
 t_{clk} &= t_{skew} + t_{clk-q, regfile} + t_{mux} + t_{alu} + t_{setup, reg} \\
 &= 1 + 2 + 1 + 5 + 1 \\
 &= 10 \text{ ns}
 \end{aligned}$$



one idea: insert registers between muxes and the ALU; remove final reg.

New critical path is from operand register through ALU and mux and back to itself:

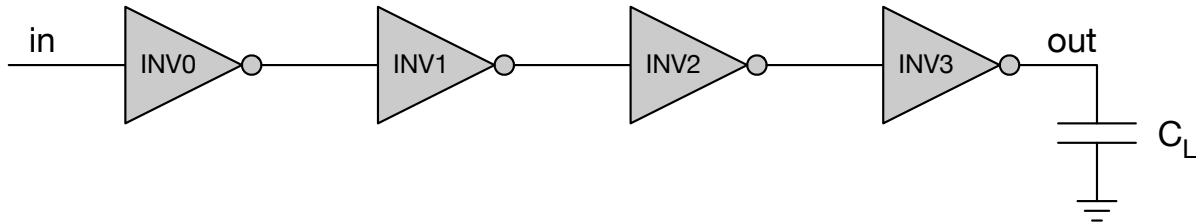
$$\begin{aligned}
 t_{clk} &= t_{skew} + t_{clk-q, reg} + t_{mux} + t_{mux} + t_{setup, reg} \\
 &= 1 + 1 + 5 + 1 + 1 \\
 &= 9 \text{ ns}
 \end{aligned}$$

This extra red line is my mistake

Problem 2: Inverter Sizing

Part a

Size inverters INV1, INV2, and INV3 in the following circuit for minimum delay. Assume $C_{INV0} = 2fF$ and $C_L = 162fF$ and that there is no interconnect capacitance.



Calculate fanout $F = \frac{C_L}{C_{INV0}} = 81$

Since there are 4 stages, the optimal fanout per stage is $f = \sqrt[4]{F} = \sqrt[4]{81} = 3$

Size each inverter relative to the first:

$$C_{INV0} = 2fF$$

$$C_{INV1} = 6fF$$

$$C_{INV2} = 18fF$$

$$C_{INV3} = 54fF$$

Part b

What is the total delay from in to out in part a? Use the simple MOSFET switch model, and assume each inverter is sized such that $R_{ON,N} = R_{ON,P}$ and $V_{th,N} = |V_{th,P}| = \frac{V_{DD}}{2}$. Assume that gate capacitance C_G and the explicit load C_L are the only sources of capacitance. R_{ON} for INV0 is $2.4k\Omega$

$$\tau_0 = R_0 \cdot C_1 = 2.4k\Omega \cdot 6fF = 14.4ps$$

$$\tau_1 = R_1 \cdot C_2 = \frac{R_0}{f} \cdot C_2 = \frac{2.4k\Omega}{3} \cdot 18fF = 14.4ps$$

$$\tau_2 = R_2 \cdot C_3 = \frac{R_0}{f^2} \cdot C_3 = \frac{2.4k\Omega}{9} \cdot 54fF = 14.4ps$$

$$\tau_3 = R_3 \cdot C_L = \frac{R_0}{f^3} \cdot C_L = \frac{2.4k\Omega}{27} \cdot 162fF = 14.4ps$$

$$t_p = \ln(2) \cdot (\tau_0 + \tau_1 + \tau_2 + \tau_3) \approx 40.0ps$$

Problem 3: Wires and Repeaters

You have two circuits on chip, A and B, that are physically located 10 mm (Manhattan distance) apart. With the following process parameters, design a chain of repeaters that minimizes the delay from A to B. Design the repeaters so that the rising and falling transitions are symmetrical. Do not worry about whether or not the signal is inverted; you may assume that the circuit B can invert the signal if needed. For your answer, include the device sizes in each repeater (including the driver inside A) and the dimensions of each wire segment.

Wire parameters:

$$R_{sheet} = 50m\Omega/\square$$

$$C_{pp} = 1.8fF/\mu m^2$$

$$C_{fringe} = 0.01fF/\mu m$$

$$W_{min} = 50nm$$

Device parameters:

$$R_{on,n} = 2k\Omega \cdot \frac{L}{W}$$

$$R_{on,p} = 4k\Omega \cdot \frac{L}{W}$$

$$\gamma = 1$$

$$L_{min} = 50nm$$

$$W_{min} = 100nm$$

$$C_{gate} = 200fF/\mu m^2$$

Start by calculating r and c :

Use a minimum length wire $W = W_{min}$

$$r = R_{sheet}/W = 50m\Omega/\square/50nm = 1\Omega/\mu m$$

$$c = C_{pp} * W + C_{fringe} = 0.1fF/\mu m$$

Size a minimum inverter:

$$W_p = 200nm \quad W_n = 100nm \quad L = 50nm$$

And calculate the drive resistance and capacitance:

$$R_d = R_{on,n} = R_{on,p} = 2k\Omega \cdot \frac{50nm}{100nm} = 1k\Omega$$

$$C_d = 200fF \cdot (0.1\mu m \cdot 0.05\mu m + 0.2\mu m \cdot 0.05\mu m) = 3.0fF$$

Now calculate the optimum number of repeaters:

$$m_{opt} = L \cdot \sqrt{\frac{0.38 \cdot r \cdot c}{0.69 \cdot R_d \cdot C_d \cdot (\gamma + 1)}}$$

$$m_{opt} = 10000\mu m \cdot \sqrt{\frac{0.38 \cdot 1\Omega/\mu m \cdot 0.1fF/\mu m}{0.69 \cdot 1000\Omega \cdot 3.0fF \cdot 2}} \approx 30$$

Now scale the inverters to size them optimally:

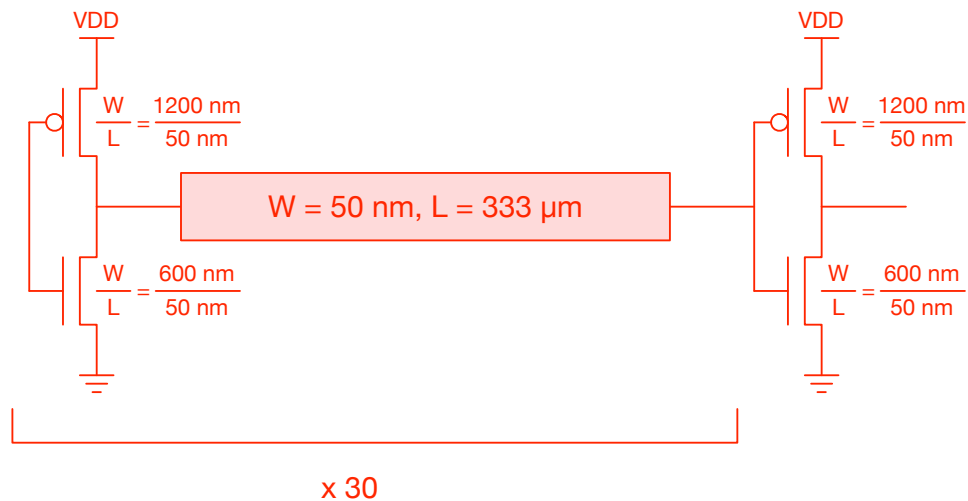
$$s_{opt} = \sqrt{\frac{R_d \cdot c}{r \cdot C_d}}$$

$$s_{opt} = \sqrt{\frac{1000\Omega \cdot 0.1fF/\mu m}{1\Omega/\mu m \cdot 3.0fF}} \approx 6$$

$$W_{n, \text{repeater}} = s_{opt} \cdot W_n = 600nm$$

$$W_{p, \text{repeater}} = s_{opt} \cdot W_p = 1200nm$$

$$L_{crit} = \frac{L}{m_{opt}} = \frac{10000\mu m}{30} \approx 333\mu m$$



We can also solve this another way (as in the lecture slides):

$$R_N = R_{on,n} \cdot L_{min} = 2000\Omega \cdot 0.05\mu m = 100\Omega \cdot \mu m$$

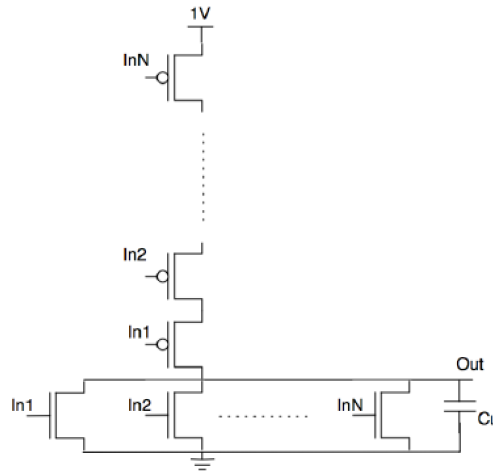
$$C_{in} = C_{gate} \cdot 3 \cdot L_{min} = 200fF/\mu m^2 \cdot 3 \cdot 50nm = 30fF/\mu m$$

$$W_{opt} = \sqrt{\frac{R_N \cdot c}{r \cdot C_{in}}} = \sqrt{\frac{100\Omega \cdot \mu m \cdot 0.1fF/\mu m}{1\Omega/\mu \cdot 30fF/\mu m}} \approx 600\mu m$$

Note that this is W_{opt} for the NMOS. The PMOS should be twice as large.

Problem 4: Power and Leakage

Consider an N-input NOR gate shown below with $V_{DD} = 1V$, $C_L = 5fF$, $C_D = 2fF/\mu m$. Assume $R_{ON,n} = 0.2m\Omega \cdot \mu m$, $R_{ON,p} = 0.3m\Omega \cdot \mu m$, $R_{OFF,n} = 100k\Omega \cdot \mu m$, $R_{OFF,p} = 1.5M\Omega \cdot \mu m$ for the given device length. You may assume $N > 2$ and you don't have to worry about extreme cases (i.e. an unreasonably large N).



a) Size the gate, using as a reference a symmetrically sized inverter with $W_n = 1\mu m$. Express your answer as a function of N.

Each NMOS has $1\mu m$ width, each PMOS has $\frac{3}{2}N\mu m$ width.

b) Assume that the probability of an input being high is 0.5 (i.e., on any given clock cycle, each input is equally likely to be a 0 or a 1.) and that all inputs are independent. What is the probability that the output is high, $P(Out = 1)$? What is the probability that the output is low, $P(Out = 0)$? What is the gate activity factor (i.e. the probability that the output will transition from low to high, $P_{0 \rightarrow 1}$)? (Again, you may express your answer as a function of N.)

$$P(Out = 1) = P(In1 = 0) \cdot P(In2 = 0) \cdot \dots \cdot P(InN = 0) = \left(\frac{1}{2}\right)^N \Rightarrow P(Out = 1) = \frac{1}{2^N}$$

$$P(Out = 0) = 1 - P(Out = 1) \Rightarrow P(Out = 0) = \frac{2^N - 1}{2^N}$$

$$a_{0 \rightarrow 1} = P_{0 \rightarrow 1} = P(Out = 0) \cdot P(Out = 1) \Rightarrow a_{0 \rightarrow 1} = \frac{2^N - 1}{2^{2N}}$$

c) What is the dynamic power dissipation of the gate as a function of N, if the clock frequency is 3GHz? You may ignore the parasitic drain capacitance in the internal nodes of the PMOS stack, but not at the output.

$$\begin{aligned}
P_{dyn} &= a_{0 \rightarrow 1} \cdot C_{L,TOT} \cdot V_{DD}^2 \cdot f \\
&= \frac{2^N - 1}{2^{2N}} (N \cdot 1\mu m \cdot C_D + \frac{3}{2} Num \cdot C_D + C_L) \cdot 1^2 V \cdot 3GHz \\
&= \frac{2^N - 1}{2^{2N}} \cdot (\frac{5}{2} N \mu m \cdot 2 \frac{fF}{\mu m} + 5fF) \cdot 1V \cdot 3GHz \\
&= \boxed{(N + 1) \frac{(2^N - 1)}{2^{2N}} \cdot 15\mu W}
\end{aligned}$$

d) **EECS 251A Only.** For the following three cases, calculate the leakage current. Express your answer as a function of N when needed. An approximate expression is perfectly fine as long as you explain and justify your assumptions/simplifications.

- All inputs are zero.

When all inputs are zero, the output is 1. All NMOS (in parallel) devices are leaking, so:

$$I_{leak,tot} = N \cdot \frac{V_{DD}}{R_{OFF,n}/1\mu m} = \boxed{10N\mu A}$$

- All inputs are 1.

When all inputs are 1, the output is 0. There is leakage through the stack of PMOS devices, so:

$$I_{leak,tot} = \frac{V_{DD}}{N \cdot R_{OFF,p}/1.5N\mu m} = \boxed{1\mu A}$$

- One of the inputs is 1, and the rest are zero.

In this case, the output is also 0. The stack of PMOS devices is leaking, but only one of them is OFF - the rest are ON.

$$I_{leak,tot} = \frac{V_{DD}}{(N - 1)R_{ON,p}/1.5N\mu m + R_{OFF,p}/1.5N\mu m}$$

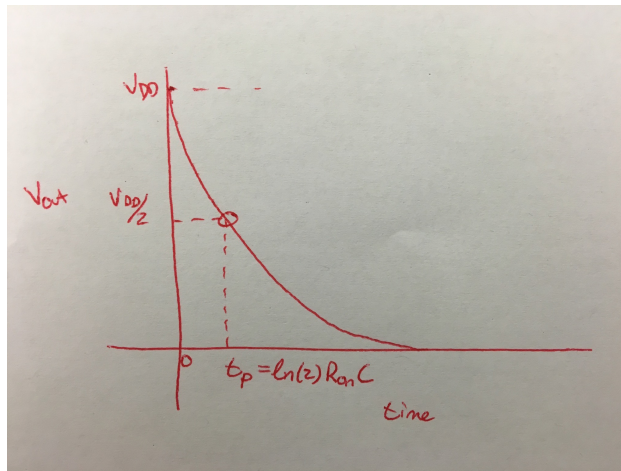
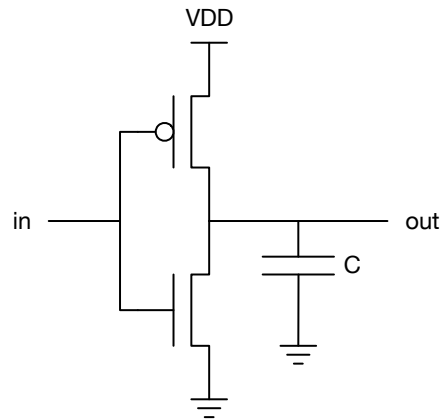
For reasonable values of N, we can assume that $R_{OFF,p}/1.5N\mu m \gg (N - 1)R_{ON,p}/1.5N\mu m$ so:

$$I_{leak,tot} \approx \frac{V_{DD}}{R_{OFF,p}/1.5N\mu m} = \boxed{N\mu A}$$

Problem 5: Gate Delays

Part a

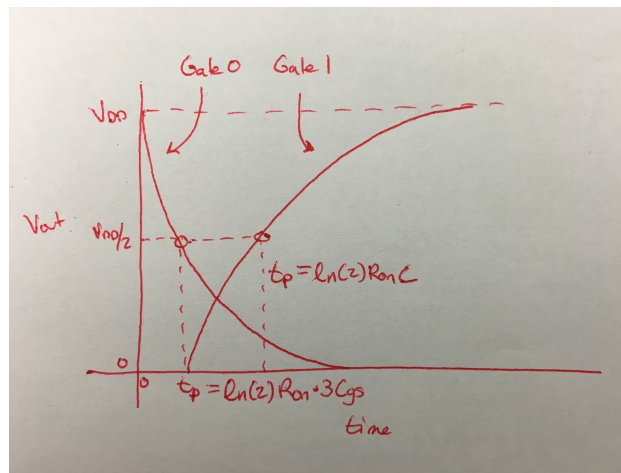
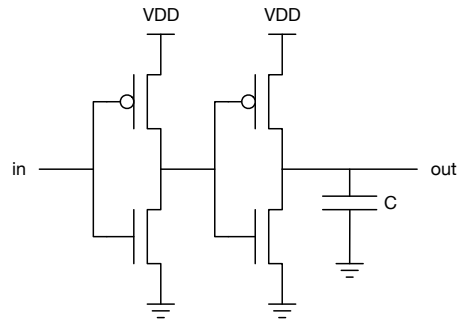
Using the transistor switch model, draw the output of the circuit below for a 0 to V_{DD} input step. Calculate the propagation delay in terms of the given parameters. Assume that $|V_{th,p}| = V_{th,n} = V_{DD}/2$ and that $R_{on,p} = R_{on,n}$. You may ignore R_{off} .



The propagation delay $t_p = \ln(2) \cdot R_{on} \cdot C$

Part b

Using the transistor switch model, draw the step response (0 to V_{DD}) of the circuit below. Calculate the propagation delay in terms of the given parameters. Assume that $|V_{th,p}| = V_{th,n} = V_{DD}/2$ and that $R_{on,p} = R_{on,n}$. Assume that $C_{gs,p} = 2 * C_{gs,n}$ and that C_{gs} is the only significant source of capacitance. You may ignore R_{off} .



The propagation delay for the first stage $t_{p,0} = \ln(2) \cdot R_{on} \cdot 3 \cdot C_{gs}$

The propagation delay for the second stage $t_{p,1} = \ln(2) \cdot R_{on} \cdot C$

The total propagation delay is therefore $t_p = t_{p,0} + t_{p,1} = \ln(2) \cdot R_{on} \cdot (3 \cdot C_{gs} + C)$