EECS 151/251A Homework 6

Due Monday, March 12th, 2018

Problem 1: RC Delay and Logical Effort Basics

Take a CMOS inverter in a process where $\gamma = \frac{C_d}{C_g}$, and the PMOS effective on-resistance is equal to K times that of the NMOS (i.e. $R_p = K \cdot R_n$) for minimally sized transistors.

(a) Draw the inverter at the transistor-level and size each FET for equal pull-up and pull-down strength. Assume the NMOS is of size '1', normalized to the minimum width of the process.

(b) Write down the delay of this unloaded inverter using RC time constants in terms of γ, R_n, and C_g. Call this delay t_p. Assume input step transitions.

(c) Now let the inverter have a load of C_L attached to it's output. Call the quantity $f = C_L/C_{in}$. Write the delay of the inverter in terms of γ, t_p, and f.

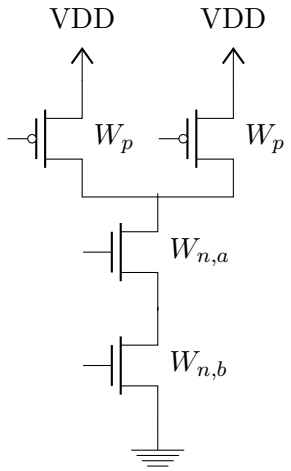
(d) Recall that the gate delay for any CMOS gate can be expressed as:

$$t_{p,gate} = t_{inv}(p + f \cdot LE)$$

where t_{inv} is a process constant, p is the intrinsic delay of the gate, and LE is the logical effort of the gate.

What are these values for an inverter?

(e) Take the following sizing of a NAND2 gate. What is W_p for inverter equivalent delay? Prove that $W_{n,a} = W_{n,b} = 2$ so the gate has equivalent self-loaded delay to an inverter and consumes minimal area.

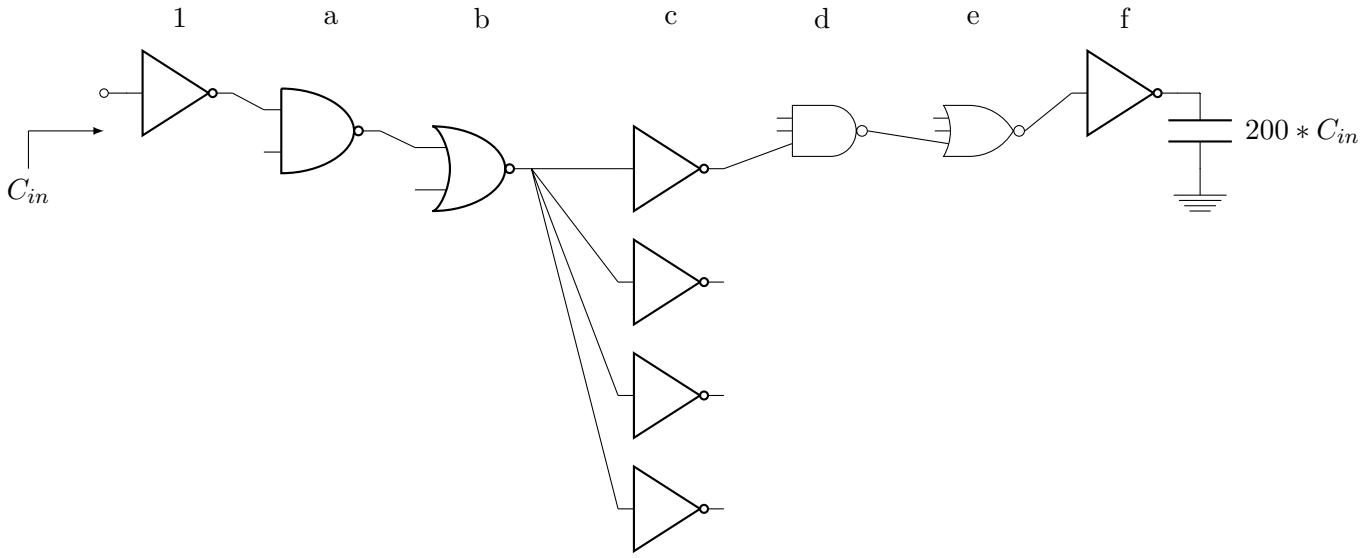


(f) Find the logical effort of this NAND2 gate for both inputs. What happens to the LE as K increases, and why does it make intuitive sense?

(g) What is the intrinsic delay of a NAND2 gate (i.e. find p_{NAND2})? Make the assumption that $K = 2$.

Problem 2: Gate Delay Optimization and Branching

Size the gates in the chain below for minimum delay. As usual, all gates are sized so that the pull-up and pull-down resistance match that of the reference inverter.



Problem 3: Voltage Scaling

To gain intuition about voltage scaling, it is important to estimate delay and energy as a function of voltage. The Alpha Power Law model of a transistor's current can estimate delay over a wide voltage range. According to that model:

$$I_{ON} \propto (V_{DD} - V_{TH})^{\alpha}$$

$$I_{OFF} \propto e^{\frac{-V_{TH}}{kT/q}}$$

Use this model with $\alpha = 1.3$, $V_{TH} = 0.3V$ and $V_{DD,nom} = 1V$ to answer the following questions about voltage scaling. Assume that at nominal supply voltage a given design runs at $1GHz$ and that the total capacitance is $C_{TOT} = 1nF$.

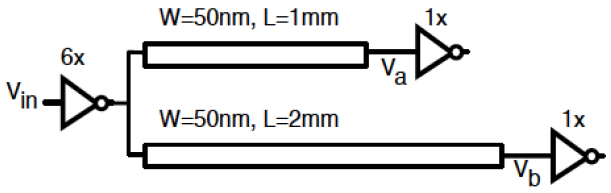
a) For $0.35V < V_{DD} < 1V$, considering dynamic energy only and an activity factor of 0.1, generate the power vs. delay (t_d) plot.

b) Now consider power as a combination of dynamic energy and leakage power. Using $I_{OFF} = 100mA$ for your given design, plot V_{DD} vs. the energy per cycle for activity factors $a = 0.1, 0.2, 0.3$. Is voltage scaling more or less effective for higher activity factors? Explain why.

Problem 4: Elmore Delay

For the following problem, $C_G = C_D = 2fF/um$, the minimum sized (labeled as 1x in the picture) inverter has $L = 0.1um$, $W_p = 2um$, $W_n = 1um$ and for this technology $R_{n,on} = 10k\Omega/sq.$ (i.e. the resistance of an NMOS with width W and length L is equal to $10k\Omega\frac{L}{W}$) and $R_{p,on} = 20k\Omega/sq.$ (i.e. the resistance of a PMOS with width W and length L is equal to $20k\Omega\frac{L}{W}$). Note that a 6x inverter has 6 times the width of a 1x inverter

For the wire, $R_{wire} = 0.1\Omega/sq.$, the parallel plate capacitance is $C_{pp} = 20aF/um^2$ and the fringing capacitance per each side of wire is $C_{fr} = 14aF/um$. The wire widths and lengths are shown in the picture.



a) Using the π wire model, draw the equivalent RC switch model. What is the propagation delay from a step at Vin to Va and Vb?

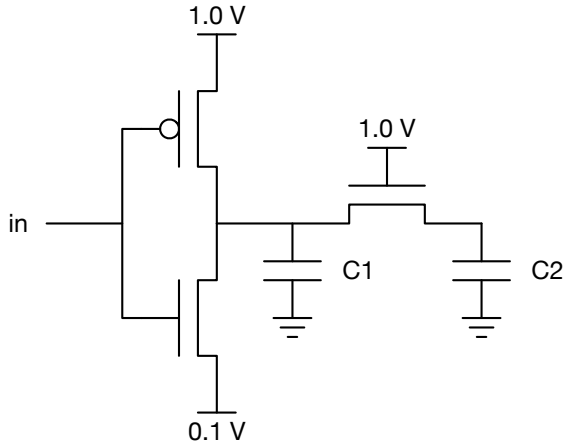
b) What is the skew (difference in arrival time between Va and Vb)?

Problem 5: Energy

Given the circuit below, answer the following questions. Assume that the capacitances associated with the FETs are negligible.

$C_1 = C_2 = 90fF$

$V_{th,n} = |V_{th,p}| = 0.4V$



Part a

How much energy is stored in each capacitor after a 1V to 0V transition on `in`? Please show your work.

Part b

How much energy was drawn by the supply in part a? Is this what you expected? Please show your work.

Part c

How much total energy is dissipated when the input goes from 1V to 0V and then back to 1V? Please show your work.

Problem 6: Processor Datapath

You are to add a *store with postincrement* instruction to a single-stage MIPS processor. The instruction **swinc** updates the index register to point to the next memory word after completing the store. **swinc $rt, imm($rs)** is equivalent to the following two instructions:

```
sw      $rt, imm($rs)
addi    $rs, $rs, 4
```

(Reminder: The first line syntax means store the word from register `$rt` to address `imm` + contents of register `$rs`.)

How would you modify the following datapath to accommodate this instruction? Try to add as little hardware as possible.