EECS 151/251A Homework 7

Due Monday, March 19th, 2018

Problem 1: Hazard Drills

Say you have a simple 3 stage in-order pipelined processor with the following stages:

1. Instruction fetch and decode
2. Execute
3. Writeback

Registers are read in the **first stage** and are written to in the third stage. Writes to registers occur at the end of a cycle while reads occur at the start.

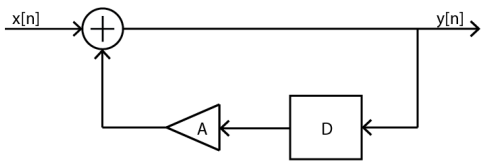
(a) Assume that data forwarding isn't implemented in this datapath. How many cycles will the following assembly take to execute?

```
add x0, x1, x2
sub x2, x3, x4
add x2, x3, x4
or  x3, x2, x0
and x4, x1, x0
xor x2, x1, x4
add x1, x2, x0
```

(b) What is the CPI of this process for this block of code?

Problem 2: Microarchitecture

In the circuit below, block D is a delay element (i.e. register) and block A performs multiplication by A.



(a) Write down the expression for $y[n]$.

(b) Unroll the loop such that each iteration covers two iterations of the original case. Substitute for $y[n-1]$ using the expression from (a) and then draw the resulting block diagram.

(c) Try to pipeline your design from part b.

Problem 3: True or False?

(a) Consider a *single-cycle* MIPS processor with only four instructions, add, sub, lw, and sw, running programs where each of the four instructions occur with equal probability. If it were practical to do so, varying the clock period on a per instruction basis would result in a overall performance improvement of at least 10%.

(b) *Multi-threading* is a known way to help eliminate hazards in pipelined processors. Instructions from multiple independent programs (or threads) are interleaved in the pipeline. This is equivalent to the "C-slow" technique we presented for optimal pipeline utilization.

Consider a standard 5-stage MIPS pipeline implementation, but with no bypassing or forwarding circuitry. Multithreading this processor with 4 independent interleaved instruction streams is sufficient to eliminate all control and data hazards.

Problem 4: DDCA Exercise 8.12

You are building an instruction cache for a MIPS processor. It has a total capacity of $4\text{C} = 2^{c+2}$. It is $N = 2^n$-way set-associative ($N \geq 8$), with a block size of $b = 2^b$ bytes ($b \geq 8$). Give your answers to the following questions in terms of these parameters:

(a) Which bits of the address are used to select a word within a block?

(b) Which bits of the address are used to select the set within the cache?

(c) How many bits are in each tag?

(d) How many tag bits are in the entire cache?