EECS 151/251A Homework 7

Due Monday, March 19th, 2018

Problem 1: Hazard Drills

Say you have a simple 3 stage in-order pipelined processor with the following stages:

1. Instruction fetch and decode
2. Execute
3. Writeback

Registers are read in the **first stage** and are written to in the third stage. Writes to registers occur at the end of a cycle while reads occur at the start.

(a) Assume that data forwarding isn't implemented in this datapath. How many cycles will the following assembly take to execute?

```
add x0, x1, x2
sub x2, x3, x4
add x2, x3, x4
or  x3, x2, x0
and x4, x1, x0
xor x2, x1, x4
add x1, x2, x0
```

Cycle	IF	EX	WB
1	add	-	-
2	sub	add	-
3	add	sub	add
4	or	add	sub
5	or	-	add
6	or	-	-
7	and	or	-
8	xor	and	or
9	xor	-	and
10	xor	-	-
11	add	xor	-
12	add	-	xor
13	add	-	-
14	-	add	-
15	-	-	add

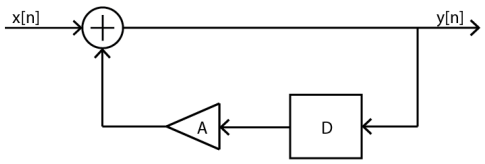
Takes 15 cycles.

(b) What is the CPI of this process for this block of code?

$$CPI = \frac{15 cycles}{7 instructions} = 2.14$$

Problem 2: Microarchitecture

In the circuit below, block D is a delay element (i.e. register) and block A performs multiplication by A.

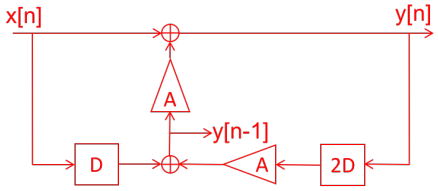


(a) Write down the expression for $y[n]$.

$y[n] = x[n] + A \cdot y[n-1]$ $\quad$ $y[n-1] = x[n-1] + A \cdot y[n-2]$

(b) Unroll the loop such that each iteration covers two iterations of the original case. Substitute for $y[n-1]$ using the expression from (a) and then draw the resulting block diagram.

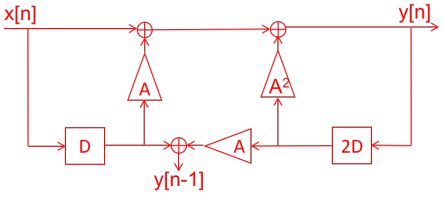
$y[n] = x[n] + A(x[n-1] + Ay[n-2])$



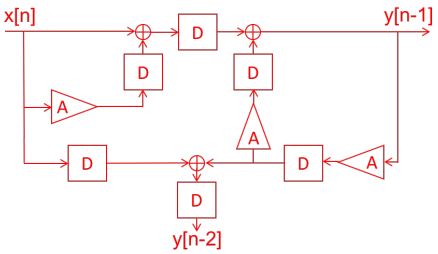
(c) Try to pipeline your design from part b.

Using distributivity and associativity:

$y[n] = x[n] + Ax[n-1] + A \cdot A \cdot y[n-2] = (x[n] + Ax[n-1]) + (A^2 y[n-2])$



Now that we have two separate loops, a pipeline register can be added in between the two adders:



Problem 3: True or False?

(a) Consider a *single-cycle* MIPS processor with only four instructions, add, sub, lw, and sw, running programs where each of the four instructions occur with equal probability. If it were practical to do so, varying the clock period on a per instruction basis would result in a overall performance improvement of at least 10%.

True

(b) *Multi-threading* is a known way to help eliminate hazards in pipelined processors. Instructions from multiple independent programs (or threads) are interleaved in the pipeline. This is equivalent to the "C-slow" technique we presented for optimal pipeline utilization.

Consider a standard 5-stage MIPS pipeline implementation, but with no bypassing or forwarding circuitry. Multithreading this processor with 4 independent interleaved instruction streams is sufficient to eliminate all control and data hazards.

True

Problem 4: DDCA Exercise 8.12

You are building an instruction cache for a MIPS processor. It has a total capacity of $4\text{C} = 2^{c+2}$. It is $N = 2^n$-way set-associative ($N \geq 8$), with a block size of $b = 2^b$ bytes ($b \geq 8$). Give your answers to the following questions in terms of these parameters:

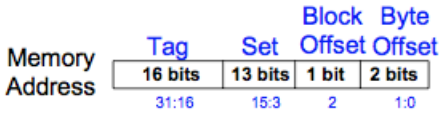
(a) Which bits of the address are used to select a word within a block?

(b) Which bits of the address are used to select the set within the cache?

(c) How many bits are in each tag?

(d) How many tag bits are in the entire cache?

(a)



(b) Each tag is 16 bits. There are 32Kwords / (2 words / block) = 16K blocks and each block needs a tag: $16 \times 16K = 2^{18} = 256$ Kbits of tags.

(c) Each cache block requires: 2 status bits, 16 bits of tag, and 64 data bits, thus each set is 2 × 82 bits = **164 bits**.

(d) The design must use enough RAM chips to handle both the total capacity and the number of bits that must be read on each cycle. For the data, the SRAM must provide a capacity of 128 KB and must read 64 bits per cycle (one 32-bit word from each way). Thus the design needs at least 128KB / (8KB/RAM) = 16 RAMs to hold the data and 64 bits / (4 pins/RAM) = 16 RAMs to supply the number of bits. These are equal, so the design needs exactly 16 RAMs for the data.

For the tags, the total capacity is 32 KB, from which 32 bits (two 16-bit tags) must be read each cycle. Therefore, only 4 RAMs are necessary to meet the capacity, but 8 RAMs are needed to supply 32 bits per cycle. Therefore, the design will need 8 RAMs, each of which is being used at half capacity.

With 8Ksets, the status bits require another 8K × 4-bit RAM. We use a 16K × 4-bit RAM, using only half of the entries.

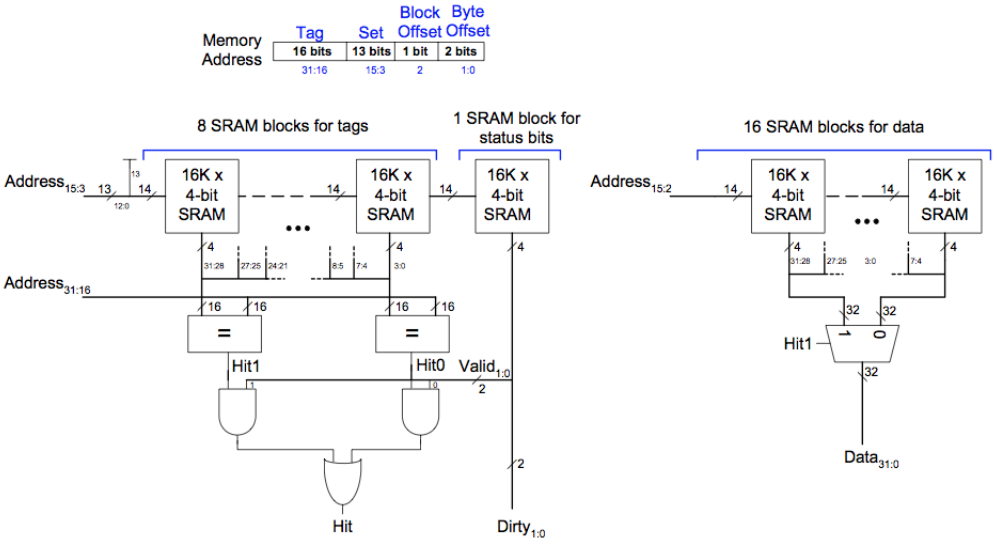


FIGURE 8.2 Cache design for Exercise 8.12

Bits 15:2 of the address select the word within a set and block. Bits 15-3 select the set. Bits 31:16 of the address are matched against the tags to find a hit in one (or none) of the two blocks with each set.