# EECS 151/251A Homework 9

Due Sunday, April 15th, 2018

## Problem 1: DDCA Exercise 8.12 :)

You are building an instruction cache for a MIPS processor. It has a total capacity of 4C = $2^{c+2}$. It is $N = 2^n$-way set-associative ($N \geq 8$), with a block size of $b = 2^{b'}$ bytes ($b \geq 8$). Give your answers to the following questions in terms of these parameters:

(a) Which bits of the address are used to select a word within a block?

(b) Which bits of the address are used to select the set within the cache?

(c) How many bits are in each tag?

(d) How many tag bits are in the entire cache?

## Problem 2: DDCA Exercise 8.13 (a) - (c)

Consider a cache with the following parameters:

- Associativity, $N = 2$
- Block size, $b = 2$ words
- Word size, $W = 32$ bits
- Cache size, $C = 32$ K words
- Address size, $A = 32$ bits

You need only consider word addresses.

(a) Show the tag, set, block offset, and byte offset bits of the address. State how many bits are needed for each field.

(b) What is the size of *all* the cache tags in bits?

(c) Suppose each cache block also has a valid bit ($V$) and a dirty bit ($D$). What is the size of each cache set, including data, tag, and status bits?

## Problem 3: True or False?

(a) The truth-table for an n-bit *carry-save adder* has exactly $2^{2n+1}$ rows.

(b) Using only 2 and 3-input CMOS logic gates, with the cost per transistor equal to 1, the minimum cost for the carry function in a full-adder cell is 16.

(c) In a 12-bit carry-select adder, grouping the bits into 3 groups of 4 bits each (4-4-4) results in lower overall delay than with any other arrangement of group sizes. Assume that the delay through a 2-input multiplexor is the same as the delay through a full-adder cell.

(d) Consider the design of a "2-bit-wide" serial adder used for adding 2 N-bit numbers (N is guaranteed to be even and at least 2). The 2-bit-wide adder is similar to the bit-serial adder from class, except that it adds *two* bit positions from each input within one cycle, instead of one; therefore it might need a longer clock period. Your design can only use flip-flops ($\tau_{clk-to-q} = \tau_{setup} = 1ns$), and full-adder cells ($\tau_{full-adder-cell} = 2ns$).

On N-bit addition, using the 2-bit design, it is possible to achieve an add *latency* (in $ns$) less than that for the normal serial adder.

(e) As a function of the number of input bits, N, the cost in terms of total transistors of a carry-lookahead adder is $\propto N + log_2(N)$.

(f) You are requested to perform a multiplication of 2 N-bit numbers, but your multiplication circuit only accepts N/2 bit wide inputs. You also have an adder circuit (of whatever width needed). The total number of times you will need to use the multiplier for the N * N multiplication is 3.

## Problem 4: The Multiplier in a Homework

(a) Draw a wallace tree for a 5 x 5 multiplier using Full Adder and Half Adder cells. What is the critical path?

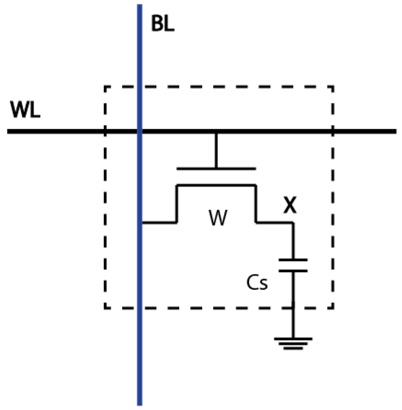
(b) Add one pipeline stage to improve the throughput as much as possible. What is the new critical path?

## Problem 5: The Multiplier in an Exam

Consider the design of a combinational **signed** 2-bit multiplication circuit. It takes as inputs two 2's complement integers, A and B, and outputs the appropriate number of result bits. Using full-adder cells (FA) and simple logic gates, draw a circuit that implements this function.

## Problem 6: DRAM Design

The figure below shows a $1\mu m \times 1\mu m$ DRAM cell with NMOS width $W = 0.5\mu m$ and $Cs = 55fF$. Assume that $C_D = C_G = 1fF/\mu m$, $V_{DD} = 1V$, $V_{TH} = 0.2V$, $I_{leak,n} = 1nA$ for a $W = 0.5\mu m$ device, that the cell is arranged in a $128 \times 8$ memory block and the wordline and bitline wires have a capacitance of $C_w = 0.2fF/\mu m$ (i.e. 0.2fF per unit length). Each bitline is connected to a sense



amplifier with $\Delta V_{sense} = 100mV$ and input capacitance 5fF, and you may ignore loading from any other peripheral circuitry. Use the ideal switch model for the transistor.

(a) WRITE: Assume the cell initially stores a "0". In order to write a "1", BL and WL are raised to $V_{DD}$. What is the final value on node X? Recommend a way to reduce the charge loss on node X without changing the cell size. Discuss the trade-offs.

(b) READ: Going back to the original array (i.e. ignoring any alterations you recommended in part a), after storing values in your memory you pre-charge the bitline to $V_{DD}/2$ and read. What is the final value on the bitline when you are reading a "1" and when you are reading a "0"?

(c) RETENTION: Calculate how often we need to refresh the memory in order to maintain its contents during retention. You may assume that the bitline is held at $V_{DD}/2$.

(d) One way to reduce power dissipation during retention is to reduce the retention frequency. Recommend a way to do that without changing the cell size. Discuss the trade-offs. *Hint:* A more realistic model for leakage is $I_{leak} \propto e^{\frac{V_{GS}-V_{TH}}{kT/q}}$.