EECS 151/251A
Midterm 2 Review

- Noise margins
  - Definitions and calculations based on transfer curves
- Logic Delay
  - RC models of gate rise/fall times and logic delay
  - Effect of transistor sizing on gate delay
  - Transistor sizing and staging for driving large capacitive loads
- Logical Effort
  - Definitions and calculation of LE for logic gates
  - LE method for optimal transistor sizing in cascades logic
  - LE method with branching
- Wire Delay Modeling
  - Distributed RC
  - Buffer insertion and effect on delay
  - Elmore delay calculations
- Delays in master/slave flip-flops
- Effect of clock skew on max clock frequency
- Retiming for optimizing clock frequency
- Power & Energy
  - Formulation of dynamic and static power consumption in CMOS
  - Voltage scaling and parallelism and pipelining for improving energy efficiency
  - Other techniques for power savings: clock gating, power gating, use of
  - High V_t transistors
- MIPS single cycle and pipelined processor organizations
  - Forwarding and stalling for hazard resolution

- Data transfers and flow-control concepts
  - Valid/Ready interface
  - Unit decoupling with FIFOs
  - FIFO operation and implementation concepts
  - Clock synchronization basics (metastability issue and simple synchronizer circuit)
- Parallelism
  - Reduction trees
  - Pipelining computation graphs (with and without feedback)
  - C-slow technique for pipelining feedback paths
  - SIMD parallelism concept
- List Processor Design Example
  - From algorithm to datapath (and control)
  - performance optimizations
- SRAM & DRAM
  - Cell operation
  - Block organization and operation