University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

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Project Report

A short final report is due by 5PM on Wed 5/9. The report should be around 8 pages total, perhaps around 5 pages of text and 3 pages of figures (plus or minus a few pages on each). Better reports mix the text and figures together.

Here is a suggested outline and page breakdown for your report. You do not need to strictly follow this outline, it is here just to give you an idea of what we will be looking for.

1. **Project Functional Description and Design Requirements.** Describe the design objectives of your project. You don't need to go into details about the RISC-V ISA, but you need to describe the high-level design parameters (pipeline structure, memory hierarchy, etc.) for this version of the RISC-V. ($\approx$ 0.5 page)
2. **High-level organization.** How is your project broken down into pieces. Block diagram level-description. ($\approx$ 1 page)
3. **Detailed Description of Sub-pieces.** Describe how your circuits work. Concentrate here on novel or non-standard circuits. Also, focus your attention on the parts of the design that were not supplied to you by the teaching staff. For instance, describe the details of your cache design. ($\approx$ 2 pages)
4. **Status and Results.** What is working and what is not? This section is particularly important for non-working designs (to help us assign partial credit). ($\approx$ 1 page)
5. **Division of Labor. This section is mandatory.** How did you organize yourselves as a team. Exactly who did what? ($\approx$ 0.5 pages)
6. **Conclusions.** What have you learned from this experience? How would you do it different next time? ($\approx$ 1 page)

When we grade your report, we will grade for clarity, organization, and grammar. Make sure to proofread and correct mistakes before turning it in.

Please turn-in your report as a PDF file—*no other formats please.*

To submit your report, check-in a file called "report.pdf" in the top-level of your design repository.