UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering and Computer Sciences
CS150 Fall 2001

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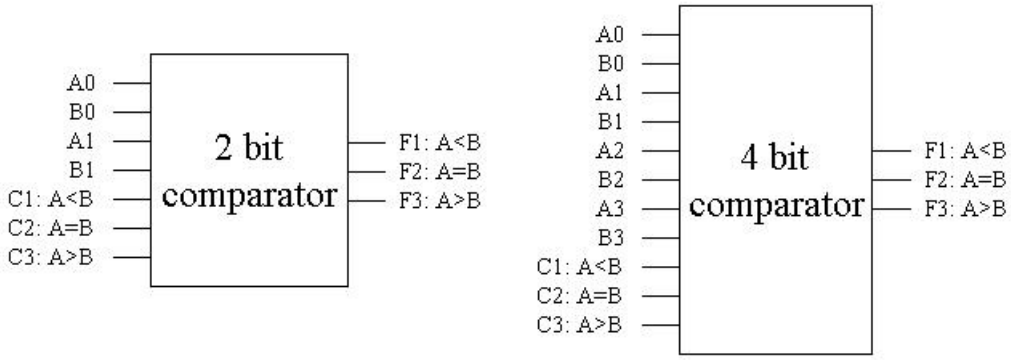
Homework #7

Due: Friday, November 16, 2001

1. A comparator with cascaded inputs uses the result of a comparison of lower order bits along with the higher order bits and determines the result of the whole comparison.
   a. Design the logic circuitry for a 2-bit comparator with cascading inputs. The inputs and outputs are show in the figure below.
   b. Design the logic circuitry for a 4-bit comparator with cascading inputs by cascading the 2-bit comparator you designed in part (a).



2. Implement a combinational logic circuit that converts a 4-bit sign and magnitude number into its corresponding 2's complement representation. Draw an input/output conversion truth table, intermediate K-maps, and your minimized two-level logic description.

3. Design a combinational circuit with an unsigned 3-bit input (A2:0), an unsigned 2-bit input (B1:0) and an unsigned 3-bit output (C2:0). Your circuit should compute the quotient of dividing A by B. For example, if A = 111b (7d) and B = 10b (2d), then C = 011b (3d), since 7/2 is 3.5, so the quotient part is 3. *Note:*Division byzero will never occur – take adbvantage of don't care conditions in this case.
   a. Write out the truth table for this circuit.
   b. Simplify the logic for C0 using a K-map.

4. The truth table for a 1-bit combinational binary subtractor, analogous to the half adder, computing D(ifference) = A minus B, with BL (borrow-from-left), is

A	B	D	BL
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

a. Design a 1-bit combinational binary subtractor, comparable to the full adder, with two data inputs (A, B), a borrow from the right input (BI), a borrow request to the left output (BL), and a difference output (D)
b. Show how your design can be cascaded to form multibit subtractors.
c. Does the subtractor work correctly for negative two's complement numbers?
d. How is a subtraction underflow condition indicated?

5. Given some 4-bit shift registers (74184's) and some full adders design a circuit that will take two four bit numbers (A3:0 and B3:0) serially (bit order: A3, A2, A1, A0, B3, B2, B1, B0) and compute the result their addition.