EECS150 - Digital Design
Lecture 2 - CMOS

August 29, 2002
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Outline

• Overview of Physical Implementations
• CMOS devices
• Announcements/Break
• CMOS transistor circuits
  – basic logic gates
  – tri-state buffers
  – flip-flops
    • flip-flop timing basics
    • circuits
    • example use
Overview of Physical Implementations

The stuff out of which we make systems.

• Integrated Circuits (ICs)
  – CL, memory elements, analog interfaces.
• Printed Circuits (PC) boards
  – substrate for ICs and interconnection, distribution of CLK, Vdd, and GND signals, heat dissipation.
• Power Supplies
  – Converts line AC voltage to regulated DC low voltage levels.
• Chassis (rack, card case, ...)
  – holds boards, power supply, provides physical interface to user or other systems.
• Connectors and Cables.
Integrated Circuits

- Primarily Crystalline Silicon
- 1mm - 25mm on a side
- 100 - 200M transistors
- (25 - 50M "gates")
- 3 - 10 conductive layers
- 2002 - feature size \( \sim 0.13\text{um} = 0.13 \times 10^{-6}\text{ m} \)
- "CMOS" most common - complementary metal oxide semiconductor

Chip in Package

- Package provides:
  - spreading of chip-level signal paths to board-level
  - heat dissipation.
- Ceramic or plastic with gold wires.
**Printed Circuit Boards**

- fiberglass or ceramic
- 1-20 conductive layers
- 1-20in on a side
- IC packages are soldered down.

**Multichip Modules (MCMs)**

- Multiple chips directly connected to a substrate. (silicon, ceramic, plastic, fiberglass) without chip packages.
Integrated Circuits

• Moore’s Law has fueled innovation for the last 3 decades.

• “Number of transistors on a die doubles every 18 months.”
• What are the side effects of Moore’s law?
Integrated Circuits

- Uses for digital IC technology today:
  - standard microprocessors
    - used in desktop PCs, and embedded applications
    - simple system design (mostly software development)
  - memory chips (DRAM, SRAM)
  - application specific ICs (ASICs)
    - custom designed to match particular application
    - can be optimized for low-power, low-cost, high-performance
    - high-design cost
  - field programmable logic devices (FPGAs, CPLDs)
    - customized to particular application
    - short time to market
    - relatively high part cost
  - standardized low-density components
    - still manufactured for compatibility with older system designs
CMOS Devices

- MOSFET (Metal Oxide Semiconductor Field Effect Transistor).

**Top View**

```
  polysilicon
     ↑   ↓
    |   |
  W   |
    |
    L
```

**Cross Section**

The gate acts like a capacitor. A high voltage on the gate attracts charge into the channel. If a voltage exists between the source and drain a current will flow. In its simplest approximation the device acts like a switch.

- **nFET**
  
  \[
  V_{gs} = '0' \\
  \]

- **pFET**
  
  \[
  V_{gs} = '1' \\
  \]
Announcements

If you are on the wait list and would like to get into the class you must:

1. Turn in an appeal for on third floor Soda
2. Attend lectures and do the homework, the first two weeks.
3. In the second week of classes, go to the lab section in which you wish to enroll. Give the TA your name and student ID.
4. Later, we will process the waitlist based on these requests, and lab section openings.

• **Please note:** Monday evening lab section will not be held (labor day). It will be held Thursday (5-8pm) evening instead.
Announcements

◆ Reading assignment for this week.
  ◆ All of chapter 1
  ◆ Chapter 10 sections 1, 2, 7, 8, 9

◆ Homework exercise is posted.

◆ Questions about class policy etc. covered on Tuesday?
Transistor-level Logic Circuits

• Inverter (NOT gate):

• NAND gate

• Note:
  – out = 0 iff both a AND b = 1 therefore out = (ab)’
  – pFET network and nFET network are duals of one another.

How about AND gate?
Transistor-level Logic Circuits

Simple rule for wiring up MOSFETs:

- nFET is used only to pass logic zero:

- pFet is used only to pass logic one:

Note: This rule is sometimes violated by expert designers under special conditions.
Transistor-level Logic Circuits

- NAND gate
- NOR gate

Note:
- out = 0 iff both a AND b = 1 therefore out = (ab)'
- Again pFET network and nFET network are duals of one another.
- Other more complex functions are possible. Ex: out = (a+bc)’
Transistor-level Logic Circuits

- Tri-state Buffer

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<th>OUT</th>
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“high impedance” (output disconnected)

- Variations

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- Transistor circuit

```
  in
   en
   en
     out
```

```
  in
   en
   en
     out
```

Fall 2002

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Transistor-level Logic Circuits

- Multiplexor

If \( s=1 \) then \( c=a \) else \( c=b \)

- Transistor Circuit
D-type edge-triggered flip-flop

- The edge of the clock is used to sample the "D" input & send it to "Q" (positive edge triggering).
  - At all other times the output Q is independent of the input D (just stores previously sampled value).
  - The input must be stable for a short time before the clock edge.

"setup" time
Parallel to Serial Converter Example

\[ \text{LD} \quad \text{X} = [x_{n-1}, x_{n-2}, \ldots, x_1, x_0] \]

• Operation:
  - cycle 1: load x, output \( x_0 \)
  - cycle i: output \( x_i \)

• Each stage:

• 4-bit version:

\[ \begin{align*}
\text{LD} & \quad \text{xi} \\
\text{FF} & \quad \text{clk}
\end{align*} \]
Parallel to Serial Converter Example

- timing:

```
clk
LD
out
x0  x1  x2  x3
```
Transistor-level Logic Circuits

• Level-sensitive latch

```
D  Q
  C
```

```
CLK
D
Q
```

• Edge-triggered flip-flop

```
D  Q
  C
```

```
D  Q
  C
```

```
clk
```

```
clk
```

```
clk
```

```
clk
```

```
clk
```

```
clk
```

```
clk
```