Homework #8

This homework is due on **Wednesday October 30th by 5pm**. Homework will be accepted in the EECS150 box outside of 125 Cory. The solution will be posted at that time. No late homework will be accepted. Please write your lab section number on your homework.

1. Write a *structural* Verilog description of a 16-bit binary counter with RST and CE inputs, and TC and count value outputs, as described in class. For this problem you may assume that a counter with delay proportional to the number of counter bits is acceptable.

2. Repeat #1 but write a *behavioral* Verilog description instead of a structural description.

3. Write a description of a 32-bit counter based on instantiations of your solution from #2.


5. Draw a block diagram of a 24-bit shifter implemented using Xilinx Virtex LUTs. Use as few LUTs as possible.

6. Consider the design a serial-to-parallel converter with a serial bit stream arriving at 64 MHz and an output stream of Bytes at 8 MHz. Sketch how to implement this based on a Xilinx Virtex BlockRam and any necessary additional circuitry — for instance one or more counters. Show all connections and label all inputs and outputs.

7. Ignoring writes, compute the maximum read bandwidth (bits per second) for the Calinx SDRAM (32-bit wide interface), assuming a 100 MHz clock.

8. Draw the circuit diagram for the FIFO design presented in class. You may abstract the combinational logic with a box labeled “CL”.