Outline

• Announcements/reminders
• List of exam topics
• Detailed discussion of quizzes and homework assignments

Please ask questions throughout!

Announcements/Reminders

• Note: HW#8 is due Wednesday at 5pm
• Exam 2 this Friday 11/1, 5pm, 1 Pimentel
  – ~90 minutes of relatively short questions covering the full range of topics from lectures 10-18.
  – Closed book and notes
  – Homework and quiz problems are typical
  – Similar in style and format as Exam 1
• Posted:
  – Quiz solutions, homework solutions
  – HW #8 solution will be posted Wednesday evening
  – These notes
• TA exam review this Wednesday, 8pm, 10 Evans

Lecture 10

Understanding of the techniques used by logic synthesis tools to convert HDLs to circuits.

Blocking and non-blocking procedural assignments.

Specification of don't cares in combinational logic.

Conceptual and practical understanding of the issue related to accidental latch generation when synthesizing combinational logic.

Sequential logic and FSM specification.

The topics in this lecture should have taken on much more meaning for you now, given your experience in the lab. I will expect that given a Verilog module, you can derive the synthesized circuit, and likewise, given a circuit you can derive a Verilog description.
Lecture 11

Carry ripple adder design.

Technique for converting adder to add/sub circuit.

Carry-select addition technique.

Carry-lookahead addition technique.

Bit-serial addition.

Cost/performance analysis of ripple, carry-select, carry-lookahead, and bit-serial adders.

General familiarity with fast-carry logic in FPGAs.

Lecture 12

Fundamentals of hardware multiplication.

Shift-and-Add multiplier data-path and control.

Modifications to multiplication technique for 2's-complement numbers.

Structure of array (combinational) multipliers.

Carry-save addition.

Wallace-tree multiplier.

Lecture 13

Modification to multiplication technique for multiplication by a constant value.

Canonic Signed Representation and other techniques for reducing the number of 1's in the constant will not be covered.

Division will not be covered.

Lecture 14

Basics of local area networks, and structure of Ethernet frames.

Principles behind network protocol stacks.

Structure of standard hardware network-interface.

The topics in this lecture should have taken on much more meaning for you now, given your experience in the lab. I will expect that you understand how to design a circuit for receiving, parsing, and filtering packets from a PHY level network interface.
Lecture 15

Basic principles of digital video:
progressive and interlaced scanning, horizontal and vertical blanking,
and RGB versus YCbYCr pixel representation.

Principle of chroma subsampling and details of 4:2:2 and 4:2:0 schemes.

General technique for ITU601 compatible video stream generation.

Principle of frame buffer design and operation.

The topics in this lecture should have taken on much more meaning for
you now, given your experience in the lab. I will expect that you
understand how to design a circuit for sending video to the encoder,
understand what is needed to design a frame buffer, and have thought
about CIF to ITU601 video transcoding.

Lecture 16

Standard internal memory organization and operation.
Details of using column muxes to control aspect ration of cell array.

Cascading memory modules to make wider or deeper memories.

Types of memories (DRAM, ROM, ...), Characteristics of S- versus DRAM.

Interface, operation, and internal organization of multi-ported memories.

Specification of memories in Verilog.

Virtex LUTs as memory blocks. Details of Virtex BlockRAMs.

Relationship between combinational logic and memory blocks.
Using ROM to implement combinational logic.
Structure and use of PLA and PLD.

Lecture 17

Details of reading and writing SDRAM.

Principles behind and details in design of FIFO memory.

Lecture 18

Design and operation of bit-serial multiplier.

Using counters with FSMs for controller implementation.

Toggle flip-flop function and design.

Structure of ripple counters.

Design of binary counters. Modification to increase max clock frequency.

Design of up/down counters.

Techniques for counting to non-power of 2 value.

Design of ring counters.