Outline

• Moore versus Mealy style state machines.
• FSM optimization
  – State Reduction
  – State Assignment
Finite State Machines

• Example: Edge Detector
  Bit are received one at a time (one per cycle), such as: 000111010 $\rightarrow$ time

Design a circuit that asserts its output for one cycle when the input bit stream changes from 0 to 1.

Try two different solutions.
State Transition Diagram Solution A

<table>
<thead>
<tr>
<th>IN</th>
<th>PS</th>
<th>NS</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00</td>
<td>00</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>00</td>
<td>01</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>01</td>
<td>11</td>
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<tr>
<td>0</td>
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<tr>
<td>1</td>
<td>11</td>
<td>11</td>
<td>0</td>
</tr>
</tbody>
</table>

IN = 0
ZERO OUT = 0
CHANGE IN = 0 IN = 0
ONE OUT = 1
IN = 1

IN = 1
ONE OUT = 0
IN = 1

IN = 1
ZERO OUT = 0
CHANGE IN = 0
ONE OUT = 1
IN = 1
Solution A, circuit derivation

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**ZERO**

**CHANGE**

**ONE**

\[ NS_1 = IN \quad PS_0 \]

\[ NS_0 = IN \]

\[ OUT = \overline{PS_1} \overline{PS_0} \]
Solution B

Output depends non only on PS but also on input, IN

Let ZERO = 0, ONE = 1

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<td>1</td>
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NS = IN, OUT = IN PS'

What’s the intuition about this solution?
Edge detector timing diagrams

- Solution A: output follows the clock
- Solution B: output changes with input rising edge and is asynchronous wrt the clock.
FSM Comparison

Solution A
Moore Machine
- output function only of PS
- maybe more states
- synchronous outputs
  - no glitches
  - one cycle “delay”
  - full cycle of stable output

Solution B
Mealy Machine
- output function of both PS & input
- maybe fewer states
- asynchronous outputs
  - if input glitches, so does output
  - output immediately available
  - output may not be stable long enough to be useful (below):

If output of Mealy FSM goes through combinational logic before being registered, the CL might delay the signal and it could be missed by the clock edge.
FSM Recap

Moore Machine

STATE
[output values]

input value

inputs

FFs

present state

next state

outputs

CL

Mealy Machine

STATE

input value/output values

inputs

FFs

present state

next state

outputs

CL

Both machine types allow one-hot implementations.
FSM Optimization

- **State Reduction:**
  
  Motivation:
  lower cost
  
  - fewer flip-flops in one-hot implementations
  - possibly fewer flip-flops in encoded implementations
  - more don’t cares in NS logic
  - fewer gates in NS logic

  Simpler to design with extra states then reduce later.

- Example: Odd parity checker.
  Two machines - identical behavior.
State Reduction

State Reduction is based on:

Two states are equivalent if, for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state.

If two states are equivalent, one can be eliminated without effecting the behavior of the FSM.

Several algorithms exist:

- Row matching method.
- Implication table method.

“Row Matching” is based on the state-transition table:

If two states have the same output, and both transition to the same next state, or both transition to each other, or both self-loop, then they are equivalent.

Combine the equivalent states into a new renamed state.

Repeat until no more states are combined.

Note: This algorithm is slightly different than the book.
Row Matching Example

State Transition Table

<table>
<thead>
<tr>
<th>PS</th>
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<th>output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x=0</td>
<td>x=1</td>
</tr>
<tr>
<td>a</td>
<td>a</td>
<td>b</td>
</tr>
<tr>
<td>b</td>
<td>c</td>
<td>d</td>
</tr>
<tr>
<td>c</td>
<td>a</td>
<td>d</td>
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<tr>
<td>d</td>
<td>e</td>
<td>f</td>
</tr>
<tr>
<td>e</td>
<td>a</td>
<td>f</td>
</tr>
<tr>
<td>f</td>
<td>g</td>
<td>f</td>
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Reduced State Transition Diagram
State Reduction

• The “row matching” method is not guaranteed to result in the optimal solution in all cases, because it only looks at pairs of states.

• For example:

```
State 0/1 1/0
S0   0/1
S1   0/1 1/0
S2   0/1
```

• Another (more complicated) method guarantees the optimal solution:

• “Implication table” method:
  See Mano, chapter 9.
State Assignment (from Katz)

• In encoded (non-one-hot) FSMs, the choice of binary encodings for the states has an influence on the number of logic gates (or LUTs) needed to compute the next state and outputs.

• For n states, at least s bits are needed for a binary encoding.

\[ s = \left\lfloor \log_2 n \right\rfloor \]

• \(2^s!\) different encodings exist.

• We will look at several “by-hand” heuristic methods for choosing good assignments.

• Some CAD tools will make assignments automatically.
• “K-maps” are used to help visualize good encodings.
• Adjacent states in the STD should be made adjacent in the map.
State Assignment

Alternative heuristics based on input and output behavior as well as transitions:

Adjacent assignments to:

- states that share a common next state (group 1's in next state map)
- states that share a common ancestor state (group 1's in next state map)
- states that have common output behavior (group 1's in output map)

Highest Priority

Medium Priority

Lowest Priority
Example: 3-bit Sequence Detector

Highest Priority: (S3', S4')

Medium Priority: (S3', S4')

Lowest Priority:
0/1, 0/0: (S0, S1', S3')
1/0, 1/0: (S0, S1', S3', S4')
Example

**Paper and Pencil Methods**

\[
\begin{array}{cc}
Q0 & 0 & 1 \\
0 & S0 & S1' \\
1 & S3' & S4'
\end{array}
\]

- Reset State = 00
- Highest Priority Adjacency

Not much difference in these two assignments
State Assignment Example

Another Example: 4 bit String Recognizer

Highest Priority: $2x(S1, S2)$
(S3', S4'), (S7', S10')

Medium Priority:
(S1, S2), $2x(S3', S4')$, (S7', S10')

Lowest Priority:
0/0: (S0, S1, S2, S3', S4', S7')
1/0: (S0, S1, S2, S3', S4', S7')
State Assignment

00 = Reset = S0

(S1, S2), (S3', S4'), (S7', S10') placed adjacently
State Assignment

Effect of Adjacencies on Next State Map

First encoding exhibits a better clustering of 1's in the next state map