EECS150 - Digital Design
Lecture 25 - Power

November 19, 2002
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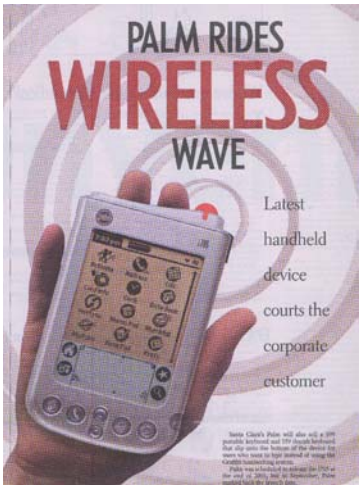
Is Power Consumption Important?



"The internet and wireless services are getting married", Simon Segars

Outline

- Motivation for design constraints of power consumption
- Power metrics
- Power consumption analysis in CMOS
- How can a logic designer control power?

Motivation

Why should a digital designer care about power consumption?

- Portable devices:
  - handhelds, laptops, phones, MP3 players, cameras, … all need to run for extended periods on small batteries without recharging
  - Devices that need regular recharging or large heavy batteries will lose out to those that don't.
- Power consumption important even in "tethered" devices.
  - System cost tracks power consumption:
    - power supplies, distribution, heat removal
  - power conservation, environmental concerns
- *In a span of 10 years we have gone from designing without concern for power consumption to (in many cases) designing with power consumption as the primary design constraint!*

Battery Technology

- Battery technology has moved very slowly
  - Moore's law does not seem to apply
- Li-Ion and NiMh still the dominate technologies
- Batteries still contribute significant to the weight of mobile devices

Nokia 61xx - 33%

Handspring PDA - 10%

Toshiba Portege 3110 laptop - 20%

Basics

- Power supply provides energy for charging and discharging wires and transistor gates. The energy supplied is stored and dissipated as heat.

$$\boxed{P \equiv dw/dt}$$

Power: Rate of work being done w.r.t time.
Rate of energy being used.

Units: $P = E/\Delta t$ *Watts = Joules/seconds*

- If a differential amount of charge dq is given a differential increase in energy dw, the potential of the charge is increased by: $V = dw/dq$
- By definition of current: $I = dq/dt$

$$dw/dt = \frac{dw}{dq} \times \frac{dq}{dt} = \boxed{P = V \times I}$$

$$w = \int_{-\infty}^{t} P dt \quad \textit{total energy}$$

Basics

- Warning! In everyday language, the term "power" is used incorrectly in place of "energy."
- Power is not energy.
- Power is not something you can run out of.
- Power can not be lost or used up.
- It is not a thing, it is merely a rate.
- It can not be put into a battery any more than velocity can be put in the gas tank of a car.

Metrics

How do we measure power consumption?

- One popular metric for microprocessors is: **MIPS/watt**
  - MIPS, millions of instructions per second.
    - Typical modern value?
  - Watt, standard unit of power consumption.
    - Typical value for modern processor?
  - MIPS/watt is reflective of the tradeoff between performance and power. Increasing performance requires increasing power.
  - Problem with "MIPS/watt"
    - MIPS/watt values are typically not independent of MIPS
      - techniques exist to achieve very high MIPS/watt values, but at very low absolute MIPS (used in watches)
    - Metric only relevant at reasonable performance range
  - One solution, **$MIPS^2$/watt**. Puts more weight on performance.

Metrics

- How does MIPS/watt relate to *energy*?
- Average power consumption = energy / time

MIPS/watt = instructions/sec / joules/sec = instructions/joule

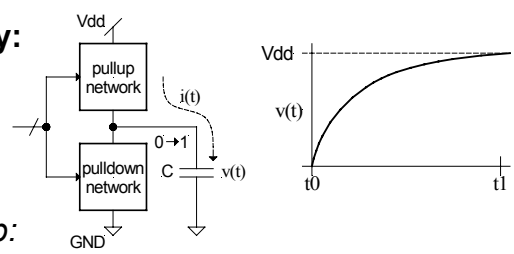
  – therefore an equivalent metric is energy per operation (E/op)

- E/op is more general - applies to more that processors
  – also, usually more relevant, as batteries life is limited by total energy draw.
  – This metric gives us a measure to use to compare two alternative implementations of a particular function.

Power in CMOS

Switching Energy:

energy used to switch a node



Calculate energy dissipated in pullup:

$$E_{sw} = \int_{t_0}^{t_1} P(t)dt = \int_{t_0}^{t_1} (V_{dd} - v) \cdot i(t)dt = \int_{t_0}^{t_1} (V_{dd} - v) \cdot c\,(dv/dt)\,dt =$$

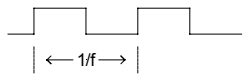
$$= cV_{dd} \int_{t_0}^{t_1} dv - c\int_{t_0}^{t_1} v \cdot dv = cV_{dd}^{\ 2} - 1/2\,cV_{dd}^{\ 2} = \boxed{1/2\,cV_{dd}^{\ 2}}$$

Energy supplied *Energy stored* *Energy dissipated*

An equal amount of energy is dissipated on pulldown.

Switching Power

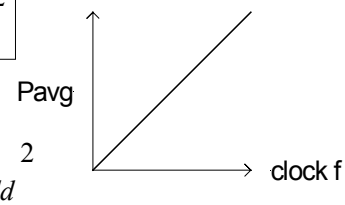
- Gate power consumption:
  - Assume a gate is switching its output at a rate of: $\alpha \cdot f$



activity factor *clock rate*

$$P_{avg} = E/\Delta t = switching\ rate \cdot E_{sw}$$

Therefore: $$\boxed{P_{avg} = \alpha \cdot f \cdot cV_{dd}^{\ 2}}$$



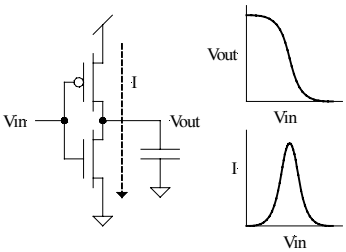
- Chip/circuit power consumption:

$$P_{avg} = n \cdot \alpha_{avg} \cdot f \cdot c_{avg} V_{dd}^{\ 2}$$

number of nodes (or gates)

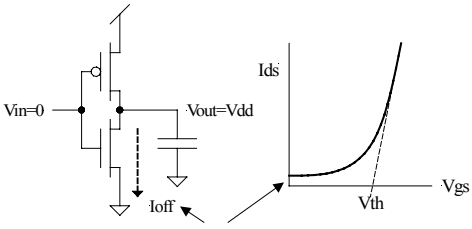
Other Sources of Energy Consumption

- "Short Circuit" Current:



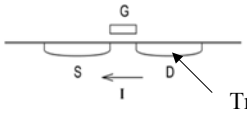
10-20% of total chip power

- Device Ids Leakage:



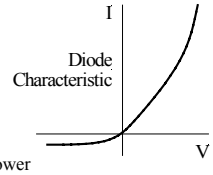
Transistor s/d conductance never turns off all the way. ~3pWatts/transistor. ~1mWatt/chip *Low voltage* processes much worse.

- Junction Diode Leakage:



~1nWatt/gate
few mWatts/chip

Transistor drain regions "leak" charge to substrate.



Controlling Energy Consumption

What control do you have as a designer?

- Largest contributing component to CMOS power consumption is switching power:

$$P_{avg} = n \cdot \alpha_{avg} \cdot f \cdot c_{avg} V_{dd}^{2}$$

  - Factors influencing power consumption:
    n: total number of nodes in circuit

    α: activity factor (probability of each node switching)

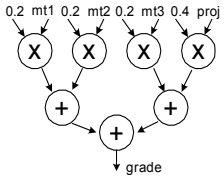
    f: clock frequency (does this effect *energy* consumption?)

    V_{dd}: power supply voltage
  - What control do you have over each factor?
  - How does each effect the total Energy?

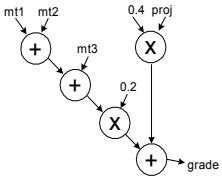
In EECS150 design projects, we will not optimize for power consumption.

Power / Cost / Performance

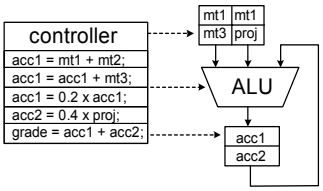
- In lecture 23 we discussed using parallelism to trade cost for performance. As we trade cost for performance what happens to energy?



$4\ E_{MUL} + 3\ E_{ADD} + E_{WIRES}$



$2\ E_{MUL} + 3\ E_{ADD} + E_{WIRES}$



$2\ E_{MUL} + 3\ E_{ADD} + E_{MUXES} + E_{CNTL} + E_{WIRES}$

- The lowest energy consumer is the solution that minimizes cost without time multiplexing operations.