EECS150 - Digital Design
Lecture 28 – Review 3

December 3, 2002
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Outline

• Announcements/reminders
• List of exam topics
• Detailed discussion of quizzes and homework assignments

Please ask questions throughout!
Announcements/Reminders

• Exam 2 this Friday evening 12/6, time/room TBA
  – ~90 minutes of relatively short questions covering the full range of topics from lectures 20-27.
  – Closed book and notes
  – Homework and quiz problems are typical
  – Similar in style and format as Exam 1 & 2
  – Attempt to make it less “challenging” and shorter. (Let me know afterwards, what you think).

• Posted:
  – Quiz solutions, homework solutions
  – HW #11 solutions will be posted today.
  – These notes

• TA exam review this Thursday, 8pm, Room TBA
Lecture 20: Finite State Machines Revisited

**Moore versus Mealy** style state machines, differences between, conversion from one to the other.

**State Reduction** using row matching method.

**State assignment** and effect on logic complexity, heuristics for good state assignments.
Lecture 21: High Level Design Part 1, Optimization of List Processor

Using register transfer level (RTL) descriptions for datapath and controller specification.

Transformation from RTL description to datapath and controller circuits.

List processing example. How the circuit works, cycle time optimization by moving operations between cycles. Analysis of relative cost and performance of various implementations.
Lecture 22: High Level Design Part 2, Scheduling

Resource utilization charts.

**Scheduling** operations on datapaths.

Highly optimized list processor implementation.

Principle and practice of *modulo scheduling* technique.
Lecture 23: High Level Design Part 3, Parallelism and Pipelining

Understanding of how to use parallelism as a way to trade-off cost for performance.

Given a computation graph (without looping) understand the range of implementations from fully parallel to sequential (time-multiplexed single operator/ALU).

Basic pipelining of combinational logic circuits. Latency versus throughput. Limits on pipelining, and ideal versus actual speedups.

Pipelining loops with feedback.

C-Slow technique.

SIMD parallelism (loop unrolling).
Lecture 24: High Level Design Part 4, CPU
Core Example

General-purpose-processor instruction set execution with datapath and control.

Details of different instructions and how they are executed.

**Microprogramming** style of controller implementation.
Lecture 25: Power

Basic definitions of power and energy.

Units (metrics) for measuring and comparing power/energy.

Switching power in CMOS at the circuit level and chip level.

How energy relates to parallelism. Power/cost/performance tradeoffs.
Lecture 26: Error Correction and LFSRs

Error checking with a single parity bit.

Construction of and use of single-error-correction Hamming code.

Use of linear feedback shift registers (LFSRs).

Relationship between LFSR circuit and primitive polynomials.
Lecture 27: Asynchronous Circuits

Asynchronous **SR-latch** construction and operation.

Level-sensitive SR-latch.

Behavior of **JK-FF**.

Importance of single point of synchronization.

Principle of synchronization failure and **metastability**.

Reliable synchronizer design.

Asynchronous **"handshake" signals** for data transfer.