Outline

• Finish up from lecture 2
• General Model of Synchronous Systems
  – Performance Limits
• Announcements
• Delay in logic gates
• Delay in wires
• Clock Skew
• Delay in flip-flops
Transistor-level Logic Circuits (cont.)

- Positive Level-sensitive latch

\[
\text{clk}'
\]

\[
\text{clk}
\]

- Transistor Level

- Positive Edge-triggered flip-flop

\[
\text{clk}'
\]

\[
\text{clk}
\]
General Model of Synchronous Circuit

- All wires, except clock, may be multiple bits wide.
- Registers (reg)
  - collections of flip-flops
- clock
  - distributed to all flip-flops
  - typical rate?
- Combinational Logic Blocks (CL)
  - no internal state
  - output only a function of inputs
- Particular inputs/outputs are optional
- Optional Feedback
Example Circuit

- Parallel to Serial Converter

- All signal paths single bit wide
- Registers are single flip-flops
- Combinational Logic blocks are simple multiplexers
- No feedback in this case.
General Model of Synchronous Circuit

• How do we measure performance?
  – operations/sec?
  – cycles/sec?
• What limits the clock rate?
• What happens as we increase the clock rate?
Limitations on Clock Rate

1 Logic Gate Delay

- What are typical delay values?

2 Delays in flip-flops

- Both times contribute to limiting the clock period.

- What must happen in one clock cycle for correct operation?
- Assuming perfect clock distribution (all flip-flops see the clock at the same time):
  - All signals must be ready and “setup” before rising edge of clock.
Example

- Parallel to serial converter:

\[ T \geq \text{time}(\text{clk} \rightarrow Q) + \text{time}(\text{mux}) + \text{time}(\text{setup}) \]

\[ T \geq \tau_{\text{clk} \rightarrow Q} + \tau_{\text{mux}} + \tau_{\text{setup}} \]
General Model of Synchronous Circuit

In general, for correct operation:

\[ T \geq \text{time}(\text{clk} \rightarrow Q) + \text{time}(\text{CL}) + \text{time}(\text{setup}) \]

\[ T \geq \tau_{\text{clk} \rightarrow Q} + \tau_{\text{CL}} + \tau_{\text{setup}} \]

for all paths.

How do we enumerate all paths?
- Any circuit input or register output to any register input or circuit output.
- "setup time" for circuit outputs depends on what it connects to.
- "clk-Q time" for circuit inputs depends on from where it comes.
Announcements

• Remember to check the web-page often.
  – Homework due Friday. Start early, get help in discussion sections and office hours.

• Look at notes online before class.
  – Suggestion: print out and bring copy to class - annotate when necessary. My notes are intentionally incomplete. Full page is easier for this than “6-up”.

• Turn in HW#1 before 1pm Friday. Homework box moving from outside 218 Cory to outside 125 Cory
  – Not sure where it will be on Friday.

• Discussions, TA office hours, and labs this week.

• Quiz Friday at lab lecture.
Qualitative Analysis of Logic Delay

• Improved Transistor Model: nFET

We refer to transistor "strength" as the amount of current that flows for a given Vds and Vgs.

• The strength is linearly proportional to the ratio of W/L.

pFET

\[ \text{Ids} \]
\[ \text{Vgs} = 2v \]
\[ \text{Vgs} = 1v \]
\[ \text{Vgs} < \text{Vth} \]

\[ -\text{Ids} \]
\[ \text{Vgs} = -2v \]
\[ \text{Vgs} = -1v \]
\[ \text{Vgs} > \text{Vth} \]
Gate Switching Behavior

- Inverter:

- NAND gate:
• Cascaded gates:

In general
prop. delay = sum of individual prop. delays of gates in series.
Gate Delay

- Fan-out:

![Diagram of logic gates with voltage over time curves showing delay]

- The delay of a gate is proportional to its output capacitance. Because, gates #2 and 3 turn on/off at a later time. (It takes longer for the output of gate #1 to reach the switching threshold of gates #2 and 3 as we add more output capacitance.)
Gate Delay

- “Fan-in”

What is the delay in this circuit?
- Critical Path: the path with the maximum delay, from any input to any output.
  - In general, we include register set-up and clk-to-Q times in critical path calculation.

Why do we care about the critical path?
Delay in Flip-flops

- Setup time results delay through first latch.
- Clock to Q delay results from delay through second latch.
In general, wire behavior as "transmission lines":
- Signal wave-front moves close to the speed of light.
- ~1ft/ns
- Time from source to destination is called the "transit time".
- In ICs most wires are short, and the transit times are relatively short compared to the clock period and can be ignored.
- Not so on PC boards.
Wire Delay

- Even in those cases where the transmission line effect is negligible:
  - Wires possess distributed resistance and capacitance
  
- Time constant associated with distributed RC is proportional to the square of the length

- For short wires on ICs, resistance is insignificant (relative to effective R of transistors), but C is important.
  - Typically around half of C of gate load is in the wires.

- For long wires on ICs:
  - Busses, clock lines, global control signal, etc.
  - Resistance is significant, therefore distributed RC effect dominates.
  - Signals are typically “rebuffered” to reduce delay:
Clock Skew

- Unequal delay in distribution of the clock signal to various parts of a circuit:
  - if not accounted for, can lead to erroneous behavior.
  - Comes about because:
    - clock wires have delay,
    - circuit is designed with a different number of clock buffers from the clock source to the various clock loads, or
    - buffers have unequal delay.
  - All synchronous circuits experience some clock skew:
    - more of an issue for high-performance pipelined designs operating with very little extra time per clock cycle.

→ ↔ clock skew, delay in distribution
Clock Skew (cont.)

- If clock period $T = T_{CL} + T_{setup} + T_{clk\rightarrow Q}$, circuit will fail.
- Therefore:
  1. Control clock skew
     a) Careful clock distribution. Equalize path delay from clock source to all clock loads by controlling wires delay and buffer delay.
     b) don’t “gate” clocks.
  2. $T \geq T_{CL} + T_{setup} + T_{clk\rightarrow Q} + \text{worst case skew.}$
- Most modern large high-performance chips (microprocessors) control end to end clock skew to a few tenths of a nanosecond.
Clock Skew (cont.)

- Note reversed buffer.
- In this case, clock skew actually provides *extra time* (adds to the effective clock period).
- This effect has been used to help run circuits as higher clock rates. Risky business!