Homework #2

This homework is due on **Friday Sep 13\textsuperscript{th} by 2pm**. Homework will be accepted in the EECS150 homework box outside 125 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is handed out.

1. **Flip-flops and timing.**

   a) For the circuit shown, assume that all the flip-flops initially hold logic 0. Draw the waveform that appears at point $y$.

   ![Circuit Diagram]

   ![Waveform Diagram]

   b) Assume the flip-flop setup time is 75ps and its clock-to-Q delay is 100ps. If the mux propagation delay is 150ps, what is the maximum clock frequency for this circuit?
2. Logic gate timing waveforms.

Below is shown the waveforms corresponding to a low-to-high and a high-to-low transition for an inverter. Draw approximate transition waveforms for the other situations shown below. Assume that all transistors in all the gates and inverters are of the same strength.

a) $V_x$ initially is high, set $a=b=\text{high}$.

b) $V_x$ initially is low, set $a=\text{high}$, $b=\text{low}$.

c) $V_x$ initially is low, set $a=b=\text{low}$.
d) Show both transitions.

\[ \tau_P = 50 + 100 \cdot f \]

where \( f \) is the fanout of the inverter, expressed in number of transistor-gate inputs (inverters contribute 2 to \( f \), one input of 2-input gates contribute 2). Assume this inverter has the same propagation delay for both low-to-high and high-to-low transitions.

The NAND gate propagation delay is expressed as:

\[ \tau_{PLH} = 100 + 75 \cdot f \]
\[ \tau_{PHL} = 100 + 125 \cdot f \]

For the low-to-high and high-to-low transitions, respectively. Write expressions for the propagation delay of the AND gate:

\[ \tau_{PLH} = \]
\[ \tau_{PHL} = \]
4. Flip-flop delay.

Consider the edge-triggered flip-flop circuit shown below. Assume that all the transistors in the flip-flop circuit are of the same size. Ignore delay due to wires. The propagation delay of the tri-state buffer and the inverter, respectively, can be expressed as:

\[
\begin{align*}
T_{TS-LH} &= 4 + 4F \quad \text{delay for tri-state buffer low to high transition} \\
T_{TS-HL} &= 2 + 2F \quad \text{delay for tri-state buffer high to low transition} \\
T_{INV-LH} &= 2 + 2F \quad \text{delay for inverter low to high transition} \\
T_{INV-HL} &= 1 + F \quad \text{delay for inverter high to low transition}
\end{align*}
\]

where \( F \) is the fan-out in units of gate inputs (one n-type and one p-type transistor gate connection). The tri-state buffer delay is the same for both the in-to-out delay and the e-to-out delay.

a) Write an expression for the clock to \( Q \) delay \( (T_{CQ}) \) of the flip-flop in terms of the fan-out of the flip-flop.
b) Determine the setup time of the flip-flop ($T_{SU}$).

c) The waveforms shown in the illustration represent the low-to-high and high-to-low transitions of a single inverter driving another single inverter. Using this as your guide, in the place provided, draw a sketch of the waveforms for both low-to-high and high-to-low transitions at node x. Assume that CLK=0.
5. Gate delay waveforms.

Consider the simple combinational logic circuit shown below. Inputs a and b are applied over three clock cycles as shown in the waveforms. The clock period is 10ns.

Don't forget to account for gate delays.