Homework #3

This homework is due on **Friday September 20th by 2pm**. Homework will be accepted in the EECS150 homework slot in the cabinet to the right of the main door into 125 Cory. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted.

1. Multi-level logic.

   a) Consider the following function expressed in two-level and/or form. Using algebraic manipulation, express the function in three-level or/and/or form:

   \[ F = ac + ad + bc + bd + e \]

   b) Now assume that you can only use two-input and and or gates to implement this function. For both the two-level and the three-level forms, determine the cost in transistors, and the delay in terms of “gate delay”.

2. From Mano: Problems 3-1, 3-8, 3-12, 3-13, 3-14, 3-15, 3-23.

3. You are a design engineer at a big automobile manufacturer and are asked to design the engine controller for the company’s new high-efficiency engine. You check around and discover that no appropriate controller already exists anywhere. You are allowed to choose one of the following: ASIC, FPGA, microprocessor. Which one would you choose and why? Discuss the issues and tradeoffs you considered.

4. Read the online Xilinx Data book (check the class website) pages 1-8. You will probably not understand everything in the data book, but do your best.

   a) Based on Figure 5 for the simplified block diagram of the slice, estimate the number of configuration bits needed to configure the internals of a slice. Remember configuration bits are used to set all internal multiplexors and fill in the tables in the LUTS. Ignore the two boxes above the lower LUT.

   b) How many block SelectRams are needed to implement a memory with 512 32-bit wide words? Alternatively, many distributed SelectRams (each distributed SelectRam is one LUTs) would be needed?
5. Draw a simple diagram that shows how you could construct a 5-LUT from a collection of 4-LUTs. Is there a simpler way to do this if you were allowed to use something in addition to 4-LUTs?

6. Given the logic function shown in the circuit below and the configurable logic block (CLB), partition the circuit so that it can be implemented with a collection of CLBs. **Try to use as few a number of CLBs as possible.** You can extend the table or leave some rows blank. If you add any new signal wires, label the wires.
7. Given the logic circuit and configurable logic block (CLB) shown below, partition the logic circuit so that it can be implemented with as little a number of CLBs as possible. Indicate your answer by filling in the table: one row per CLB used; write in the name of the signal wire from the logic circuit that corresponds to the CLB input or output; for the configuration bit, s, write in a “0” or “1”. You can leave some rows blank.