University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS150 J. Wawrzynek
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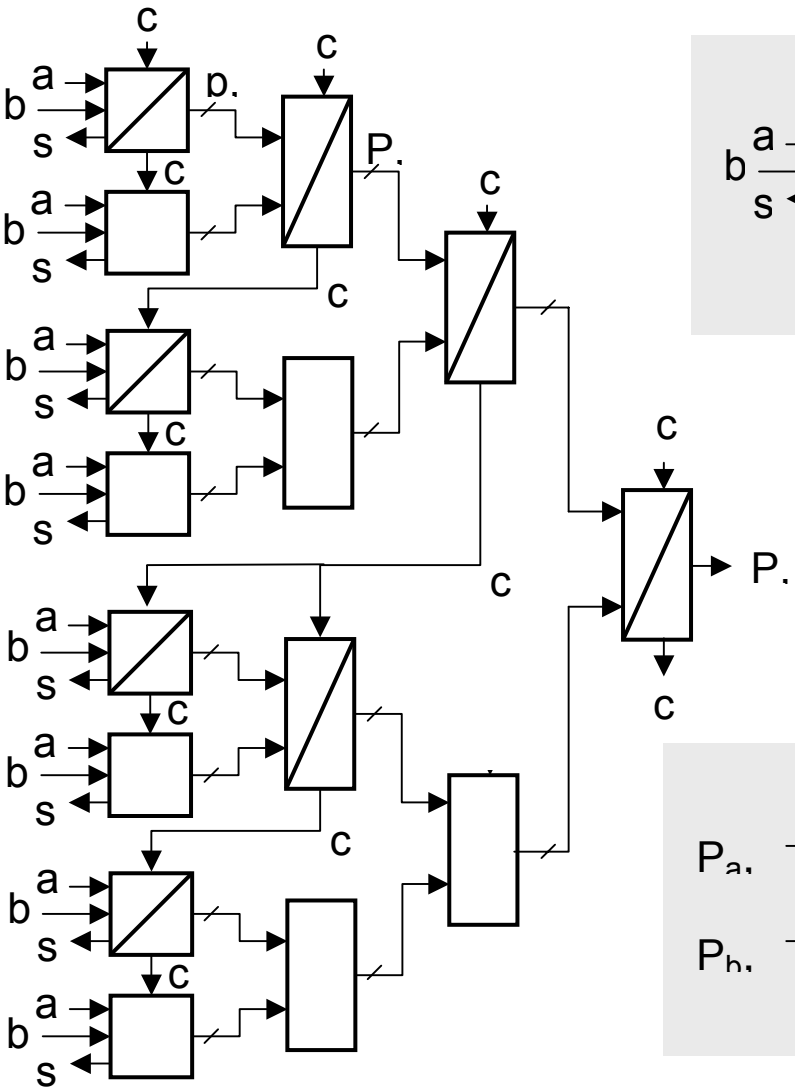
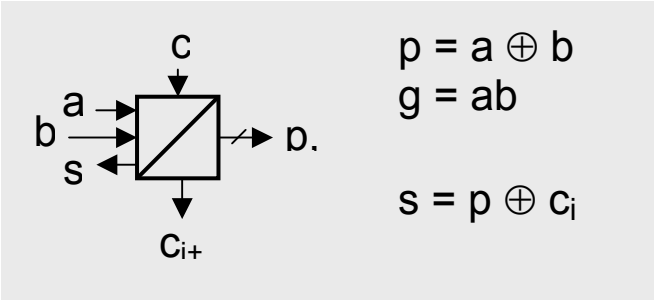
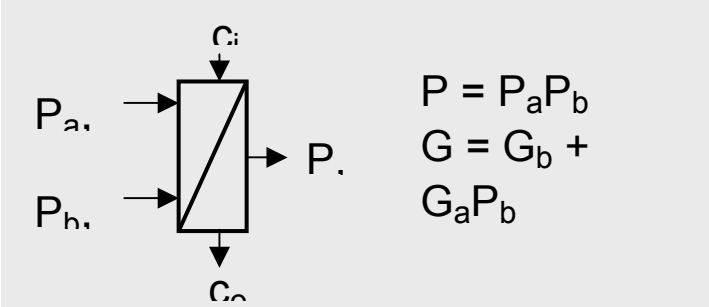
Homework #5

This homework is due on **Friday October 11th by 2pm**. Homework will be accepted in the EECS150 box outside 125 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted. Please put your lab session number on your solution.

1. Below is the illustration of the 8-bit carry look-ahead adder presented in class. Draw a line on the circuit representing the critical path (signal path with worst-case delay). Using "big O" notation, how does the delay and cost scale with n for this type of adder?







2. Ignoring the Xilinx Virtex dedicated carry-chain circuits, how many 4-LUTs would it take to map the 8-bit carry-lookahead adder illustrated above?

3. Carry select adders.

   a) In class we discussed the carry-select adders. Assuming that the select groups are all of the same number of bits, and the carry delay through a full-adder cell is equal to the delay of a 2-to-1 mux, what is the optimal size select group for a 32-bit adder?

   b) In class we also discussed the possibility of applying the carry-select idea hierarchically. The idea is that a ripple adder of n-bits can be split and implemented as a carry-select adder with group size n/2 (implemented as three ripple adders of size n/2 along with muxes). Then each of the three adders of size n/2 could be split and implemented as a carry-select adder with group size n/4, etc. By continuing the process eventually the adder size would be 1-bit and the process ends.

      Discuss the worst case delay through this adder. Again using "big O" notation, how does the delay scale with n? How does the cost (amount of hardware - number of gates or transistors) scale with n?

4. For this problem assume that your complete library of logic components comprises 2-input AND, OR, and XOR gates and inverters. Assume that inverters have cost of one unit and delay of one unit, and all other logic gates have cost of 2 units and delay of 2 units (ignore fanout and wire delay). With these assumptions, a 2-input mux would be implemented with two AND gates, one OR gate, and one inverter, and would cost 7 and have delay 5. Generate a table comparing four different adder architectures for delay and cost. The adder architectures are i) 32-bit ripple adder, ii) 32-bit carry-select adder from problem 2.a) above, iii) 32-bit hierarchical carry-select adder from problem 2.b) above, and iv)a 32-bit carry look-ahead adder based on the 8-bit carry look-ahead adder presented in class. Can you draw any conclusions from the results presented in the table?

5. Carry select adders on Xilinx Virtex. The Xilinx datasheets state that ripple-carry (using dedicated logic) is 0.05ns per stage, and the input to output delay of a 4-LUT is 0.4 ns. Ignoring wiring delay,

   a) Write a formula for the delay in a carry select adder assuming all select groups are the same size, as a function of the number of bits, n, and the select group size, r.
   b) Find an expression for r as a function of n that minimizes the delay.
   c) What is the best value for r when n=64? How about n=128.

d) If we relax the restriction that all the select groups must be the same size, what values would you use for select group sizes for n=64? How about n=128?

6. From Mano, exercises 4-10, 4-11, 4-13, 4-15 & 4-21.