a) Calculate the total cost for the 16-bit carry-select adder: 

Subdivision & duplication once yields 3 8-bit adders and 9 muxes. Subdividing once more yields 9 4-bit adders and 24 muxes. Therefore:

Total cost = 9 * 4 * Cost(FA) + 24*Cost(Mux) = 36 * 14 + 24 * 6 = 648 OR 36 * 10 + 24 * 6 = 504 depending on how the Full Adder cell was constructed.

b) Calculate the delay from \( c_{IN} \) to \( c_{OUT} \):

Delay of 4 FA ripple + delay of 2->1 mux + delay of 2->1 mux = depending on FA design,

3gates*2delay*4FA +4delay +4delay = 32 delay

OR

3gates*2delay*1FA +2gates*2delay*3FA +4delay + 4delay = 26 delay

c) In words, describe the path with the worst case delay from any of the inputs to any of the outputs:

The path from (depending on how the full adder cell is constructed) either A0/B0 to Cout, or Cin to Cout, namely, through the first 4-bit ripple, through the carryout mux 4 bits further down the chain, and through the last carryout mux 8 bits further down the chain from that.