Imagine yourself tasked with building a circuit to sum arbitrary valued lists of 8 numbers, each 8 bits wide, as quickly as possible using a set of carry-save adders (CSAs) and a single ripple adder. Use only as many CSAs as are necessary to perform the summation in minimum time.

A) In the space below, draw a diagram depicting the circuit you would construct. Draw all adders as blocks. Label each set of wires in-to and out-of an adder block with the width of the bus.

B) Assume a full adder cell has a delay of 1 unit from any input to any output. What is the worst-case delay through the circuit?

4* CSA delay + delay of 12 bit ripple adder = 4*FA delay+12*FA delay = 16 units
A) In the space below, draw a diagram depicting the circuit you would construct. Draw all adders as blocks. Label each set of wires in-to and out-of an adder block with the width of the bus.

B) Assume a full adder cell has a delay of 1 unit from any input to any output. What is the worst-case delay through the circuit?

4 CSA + 11 bit ripple = 15 units of delay