Following are some common mistakes which were seen to be made:

1. The VideoMod module has an input `rst(SW[1])`. SW[1] is an input from the button on the board, which is ACTIVE_LOW. i.e., normally the output of the switch is a high. When pressed, it goes low. All the switches on the board are active low.

2. The RESET input to the video encoder (reset output from the VideoMod) is ALSO active low. So you have to pull it down to logic low and then push it back to logic high before you set about sending \( I^2C \) and the video data.

3. Speaking of \( I^2C \), its pronounced eye-squared-see, not eye-two-see.

4. On \( I^2C \), After sending the Last byte, you have to send a 0 for a full clock cycle, before sending the stop signal (low-to-high when the clock is high). This is not explicitly specified in the section titled Testing \( I^2C \), where it the sequence is given as

   \[ S<\text{Encoder Addr}>0<\text{02 Hex}>0<\text{60 Hex}>0<\text{00 Hex}>0<\text{40 Hex}>S \]

   There is an Acknowledgement before the final S, i.e. it should be:

   \[ S<\text{Encoder Addr}>0<\text{02 Hex}>0<\text{60 Hex}>0<\text{00 Hex}>0<\text{40 Hex}>\langle 0 \rangle S \]

   And this should last for a FULL clock cycle before sending the low-to-high transition. This is also shown in the diagram in the encoder datasheet.

   ![Diagram](image)

   Last data bit sent when the clock is low
   Acknowledgement bit sent when the clock is low
   Wait for a COMPLETE clock cycle
   After that, when the clock is high the NEXT time, send a Low to High transition when the clock is high

This waiting is not required at the beginning for the start bit. This is applicable only for the STOP bit.