# EECS150: Components and Design Techniques for Digital Systems


Instructor: Prof. R. S. Fearing ronf@eecs x2-9193
Office Hours: M1-2, Tues 330-430, Thurs 10-11 in 265 M Cory.
Head TA: Alex Krasnov akrasnov@cory

| TA's: | E-mail |
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| Readers | E-mail |
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| Gerald Wang | geraldw@eecs |


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The required text is:
*Advanced Digital Design with Verilog HDL,* by M.D. Ciletti. (More basic texts are on reserve in the Engineering Library.)

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Lectures: TuTh 2-3:30 pm in 10 Evans
Lab Discussion Lecture (starts Aug. 29) F 2-3 will be in either 10 Evans or in 125 Cory depending on topic. See web page for each week's location.

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**Grading:**

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| Quiz 1 | 10% | Tue. Sep. 30 in class (tentative) |
| Quiz 2 | 10% | Thu. Nov. 6 in class (tentative) |
| Final Exam | 30% | Thu. Dec. 11, 1230-330 pm |
| Problem Sets | 10% | Due 10 am Friday in box outside 218 Cory |
| Labs 1-5 | 10% | Due within first 30 minutes of your next lab |
| Final Project | 30% | Due week of Nov. 24 |

Quizzes and examinations will cover material from lecture, discussion sections, and lab work. Any homework handed in after 10 am Fri. but before 5 pm Mon. will receive half credit otherwise due, and will not be graded after that time.

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**Laboratory:** The laboratory facilities are located in 125 Cory Hall. Labs start Tues. Sept. 2. Sections can not be changed without approval of head TA.

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**Communications:**

All class information will be stored online, available through links from the class homepage at **http://www-inst.eecs.berkeley.edu/~cs150/** . Check there for class notes, homework assignments, lab exercise handouts, and all other class materials. For notices and announcements, we will post messages to the EECS150 newsgroup (ucb.class.cs150) or send email to individuals. We will assume that everyone will have seen our postings within 24 hours of their appearance.
Staff email: **cs150@po**