Preliminary Syllabus for EECS 150, Fall 2003

Prof. Fearing

Text: M.D. Ciletti, *Advanced Digital Design with the Verilog HDL*

#	Date	Lecture Topics	Reading-Ciletti	Lab
1	26 Aug	Boolean Alg., numbers, symbols	2.1-2.3, App.A	
2	28 Aug	CMOS	3.2	
3	2 Sep	combinational logic	2.4, 2.6	Lab 1
4	4 Sep	FPGA Overview	8.9, 8.14, 8.17-8.20	Instrumentation
5	9 Sep	Hardware description language	4-4.4, 5-5.4, 5.9	Lab 2
6	11 Sep	FSM I	3-3.7, 5.5-5.8,	CAD Tool Flow
7	16 Sep	FSM II	5.10-5.16	Lab 3
8	18 Sep	HDL Synthesis/ FSM III	6-6.7	Verilog Simulation/Mapping
9	23 Sep	sequential synthesis/timing	6.9-6.15, 11-11.6	Lab 4
10	25 Sep	SDRAM/review	8.2, SDRAM data sheet	FSM Design
	30 Sep	QUIZ 1 (tentative)		Lab 5
11	2 Oct	SDRAM, cont.		Debugging
12	7 Oct	Project Description I	7.6, 4.2.5	Checkpoint 1
13	9 Oct	video interface, A/D	handouts	SDRAM I
14	14 Oct	top-down design, synch design	7.1-7.2, 7.4	Checkpoint 2
15	16 Oct	serial communications	7.4, 3.7	SDRAM II
16	21 Oct	computer data path	7.3	Checkpoint 3
17	23 Oct	computer control unit I	7.3	Video Decoder
18	28 Oct	μ programming	handout	Checkpoint 4
19	30 Oct	pipeline and FIFO	9.5-9.7	Video Encoder I
20	4 Nov	quiz review		Checkpoint 5
	6 Nov	QUIZ 2 (tentative)		Video Encoder II
	11 Nov	Veteran's Day, no lecture		Checkpoint 6
21	13 Nov	Arithmetic processors	11.2-11.4	
22	18 Nov	K maps, FSM optimization	2.4, 3.8	Checkpoint 7/early finish
23	20 Nov	metastability, arbiter, hazards	5.17, 2.5	
24	25 Nov	testability	11.7-11.9, 11.10.8	Proj. Demo deadline
	27 Nov	no lecture Happy Thanksgiving		
25	2 Dec	design example (nano)	handout	
26	4 Dec	final review		Proj. Report Due
	11 Dec	final exam Thurs 1230-330 pm		