Professor Fearing EECS150/Problem Set 10 Fall 2003

Due at 10 am, Fri. Dec. 5 in box outside 125 Cory Hall

(This problem set may be done individually or by a group of two people maximum.)

1. K-maps (20 pts)

With a four digit binary input number $A_3A_2A_1A_0$, design a circuit that generates a 3 bit output code $N_2N_1N_0$ which is the quotient of the input divided by 3. For example if the input is 13 (1101_2), $13/3 = 100_2$ thus $N_2N_1N_0 = 100_2$. a) Define the truth table for the three functions.

b) Show all Karnaugh maps for S.O.P. and P.O.S.

c) Draw the logic diagram using NAND gates only for minimized S.O.P. (Follow the bubble matching conventions).

d)Draw the logic diagram using NOR gates only for minimized P.O.S. (Follow the bubble matching conventions).

2. State Minimization (20 pts)

Given the state table below, use the state implication method to find and draw the fully reduced state diagram. (Notation for next state $IN = 0/IN = 1$.)

present state	next state	output
S0	S1/S6	0
S1	S2/S6	0
S2	S2/S3	1
S3	S4/S0	0
S4	S3/S0	0
S5	S5/S3	1
S6	S5/S1	0

3. Metastability (40 pts)

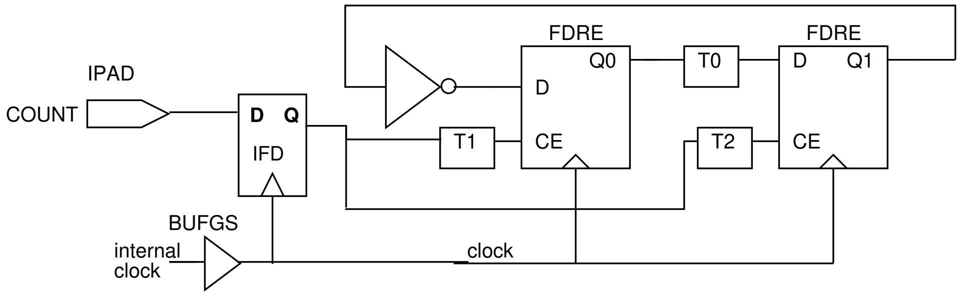
This question considers the problem of a synchronizer FF going metastable and causing an FSM to have an incorrect next state. Consider a FSM as shown in the block diagram below, using the Xilinx Virtex-II Pro. Assume COUNT (an unsynchronized input) is at 10.0 MHz and Clock is at 100.0 MHz. For this problem consider the parameters of the XC2VPro. For the CLB FF, $T_{DYCK} = T_{setup} = 0.00$ ns min, $T_{CKO} = 0.37$ ns, $T_{INV} = T_{ILO} = 0.28$ ns. Delays are $T_0 = 5$ ns, $T_1 = 7.5$ ns, and $T_2 = 7$ ns. The input FF has propagation delay $T_{IOCKIQ} = 0.60ns$.

a. Draw a detailed timing diagram for the FSM. What is the maximum metastable time Δ_O which can be tolerated without effecting proper FSM operation?

b. What is the Mean Time Between Failure for this clock and data rate? (in years)

c. Now assume that there is an additional 1.0 ns delay, so that T_2 now equals 8.0 ns. Now what would the MTBF be?

d. Your airplane flight controller company uses an FSM based on the Virtex-II Pro with 10 FF running at 100 MHz, and a 7.5 ns delay from the synchronizing IFD through the NSD to the CLB D FF inputs. The pilot provides an asynchronous input with maximum frequency of 2 Hz. Unfortunately, the FSM is not self-starting, so if any FF makes an incorrect transition, a reboot is required. If you had 1000 planes continuously flying your avionics, how often would a plane need rebooting?



4. Testability (20 pts)
Which nodes in the circuit below can not be completely tested for functionality by setting inputs ABC and observing output Y? Is the unobservable fault(s) stuck-at-one or stuck-at-zero?