Professor Fearing EECS150/Problem Set 2 Fall 2003

Due at 10 am, Fri. Sep. 12 in box outside 125 Cory Hall

Reading Ciletti: 2.4, 2.6, 3-3.2

1. (20 pts)

a. Design a 4-bit majority function using a single 8 input multiplexer and minimal extra gates (if needed). (The output should be asserted if more than half the input bits are ones.)

b. Design a 4-bit majority function using a single 4 input multiplexer and minimal extra gates.

2. Look Up Tables (25 pts)

You are given a look up table (LUT) with 3 binary inputs and one output.

a) Show how these 3 input LUTs can be combined to perform ANY 4 input logic function.

a) Show how these 3 input LUTs can be combined to perform ANY 5 input logic function.

3. Combinational Logic Design (20 pts)

a. Design a combinational circuit that will compare two bits A and B and generate 3 outputs: i) min(A,B), ii) $A < B$, iii) $A = B$, where the output will be asserted if the condition is true. This circuit must be designed such that it is modular and can be cascaded. Show truth table and logic to implement.

b. Show how to interconnect your 1 bit modules to implement a combinational logic system which will take as input two 8 bit numbers A[7:0] and B[7:0] and output 8 bits representing the minimum of A and B.

c. Assuming unit delay for all gates and inverters, calculate the worst case delay for calculating the 8 bit min.

4. D- master-slave FF Timing (35 pts)

Draw a timing diagram for the circuit below, assuming unit delay through the inverters and transmission gates, and showing signals $clk, DM, D1M, QbM, QM, D1S, QbS, QS$.