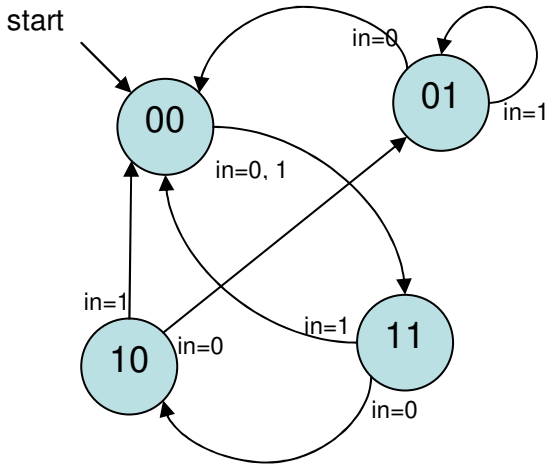
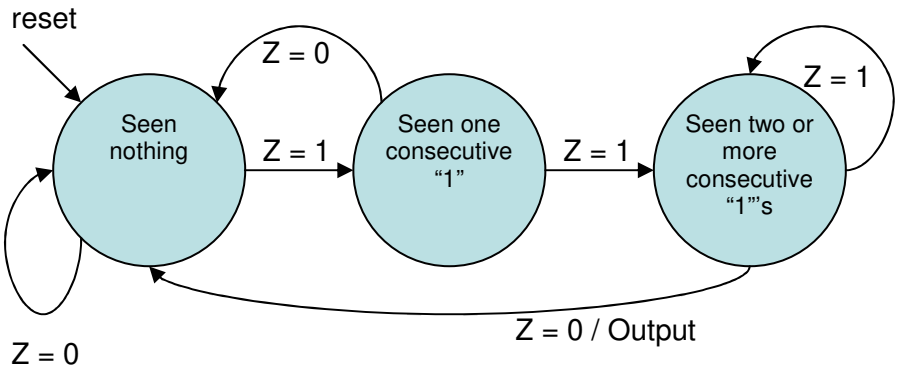
1. State transition table:

IN	Q_1	Q_0	D_1	D_0
0	0	0	1	1
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

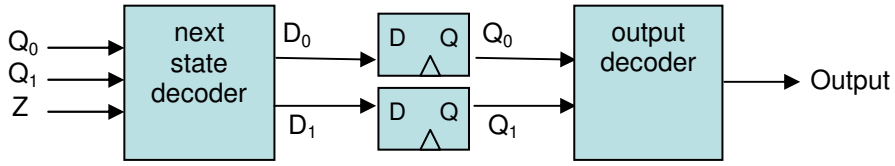
State diagram:



2. State diagram:



Block Diagram:



State encoding:

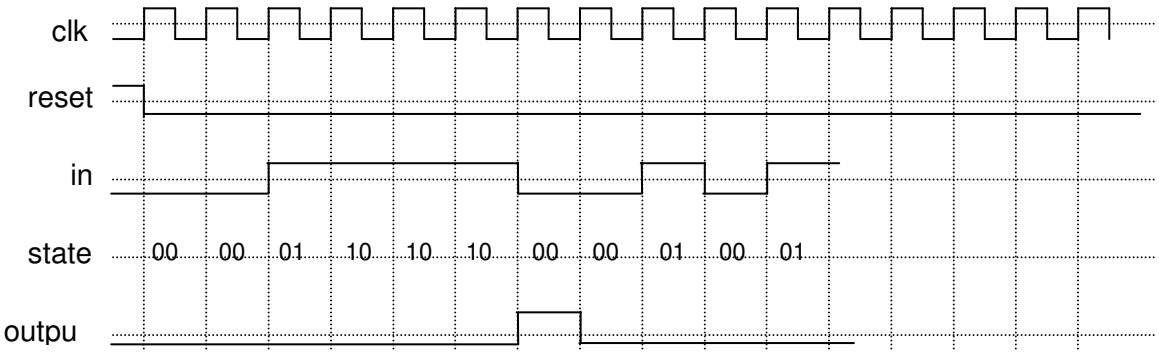
Seen nothing	00
Seen one consecutive "1"	01
Seen two or more consecutive "1"'s	10

State transition table:

Present State Q_1	Q_0	In	Next State D_1	D_0	Output
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	x	0	0	0

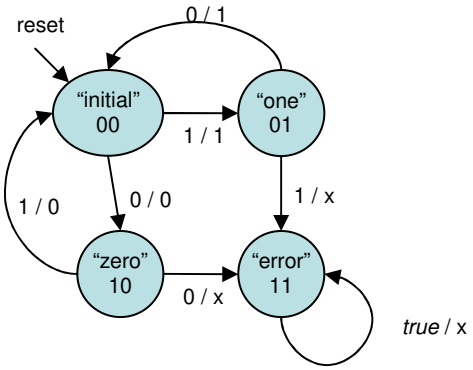
Timing diagram:

example input data sequence Z: 0, 0, 1, 1, 1, 1, 0, 0, 1, 0, 1



3. a. *Mealy machine*

State diagram:

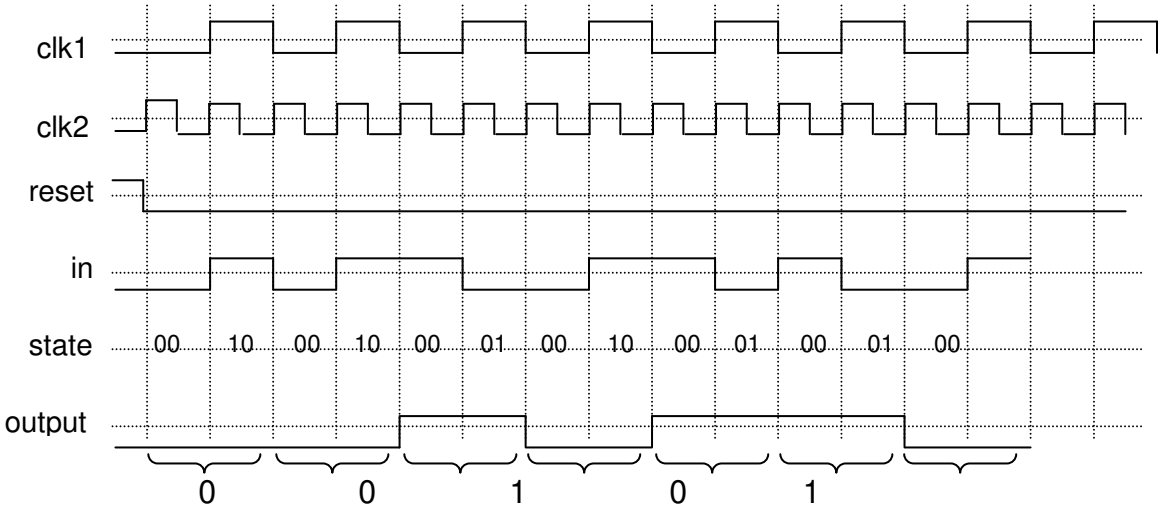


The error state is reached when an input sequence is detected that doesn't follow the rules of Manchester encoding. This isn't absolutely necessary; if you don't care about error detection and want the smallest circuit, you can make all illegal edges don't cares.

State transition table:

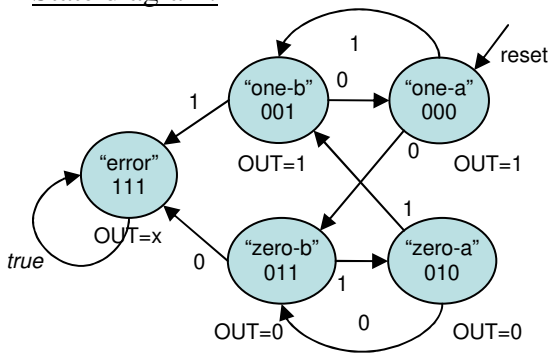
Q_1	Q_0	In	D_1	D_0	Output
0	0	0	1	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	1	x
1	0	0	1	1	x
1	0	1	0	0	0
1	1	x	1	1	x

Timing diagram:



b. *Moore machine*

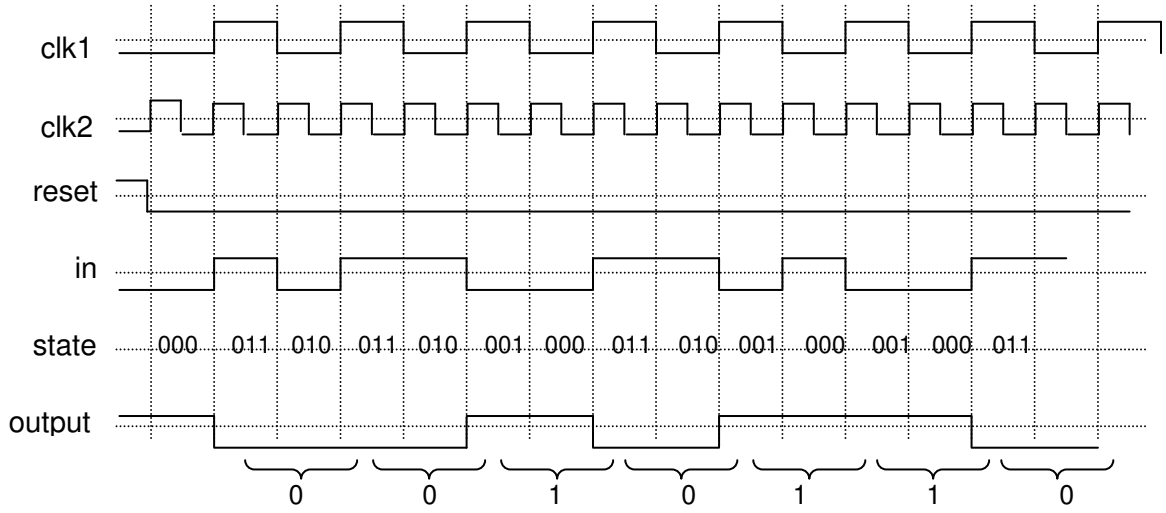
State diagram:



State transition table:

Q_2	Q_1	Q_0	IN	D_2	D_1	D_0
0	0	0	0	0	1	1
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	1
0	1	0	0	0	1	1
0	1	0	1	0	0	1
0	1	1	0	1	1	1
0	1	1	1	0	1	0
1	0	0	0	x	x	x
1	0	0	1	x	x	x
1	0	1	0	x	x	x
1	0	1	1	x	x	x
1	1	0	0	x	x	x
1	1	0	1	x	x	x
1	1	1	x	1	1	1

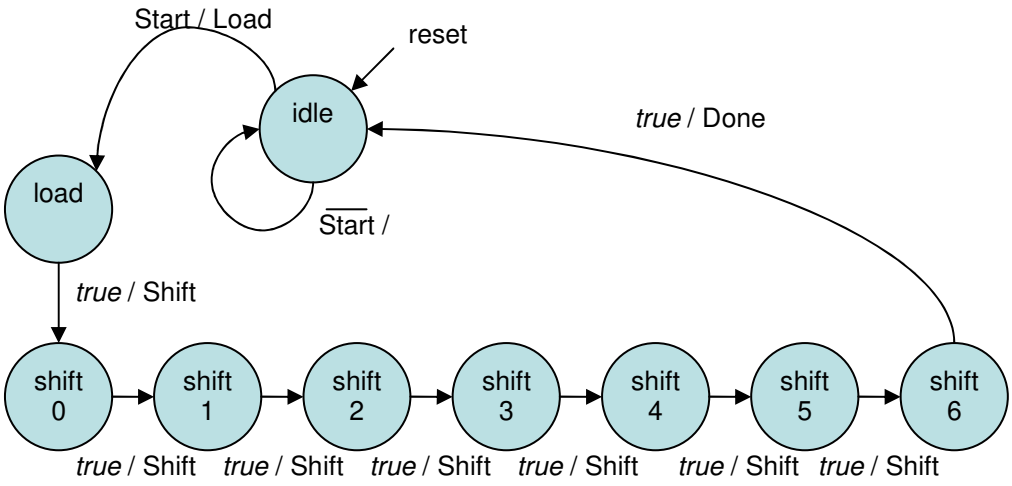
Timing diagram:



Notice that the output of the Moore machine is delayed by a clk2 cycle.

4. There is one input to our control circuit: start, there are two outputs to control the datapath: load and shift, and one control output: done. The reset do not require any nontrivial control.

State diagram:



Note that on the load, the first bit is already present on the output. Only 7 shifts are required.

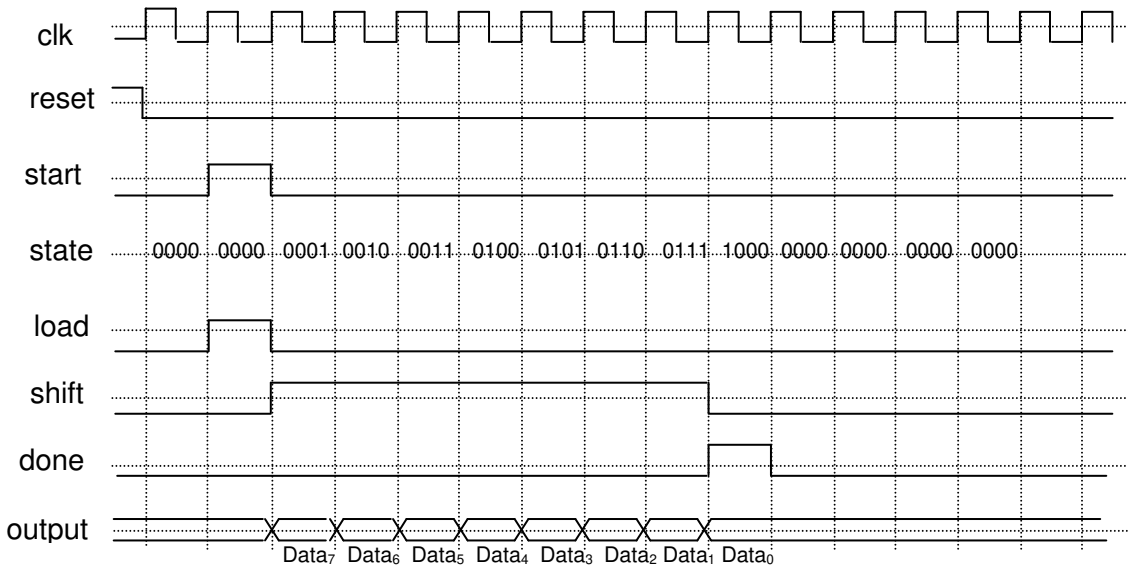
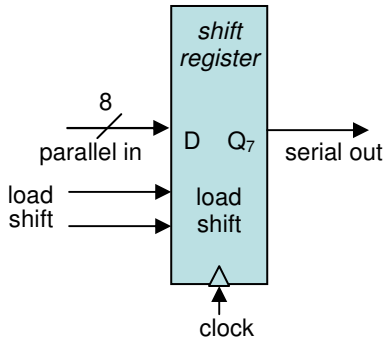
State encoding:

idle	0000
load	0001
shift 0	0010
shift 1	0011
shift 2	0100
shift 3	0101
shift 4	0110
shift 5	0111
shift 6	1000
unused	1001 through 1111

State transition table:

Q_3	Q_2	Q_1	Q_0	Start	D_3	D_2	D_1	D_0	Load	Shift	Done
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	1	0	0
0	0	0	1	x	0	0	1	0	0	1	0
0	0	1	0	x	0	0	1	1	0	1	0
0	0	1	1	x	0	1	0	0	0	1	0
0	1	0	0	x	0	1	0	1	0	1	0
0	1	0	1	x	0	1	1	0	0	1	0
0	1	1	0	x	0	1	1	1	0	1	0
0	1	1	1	x	1	0	0	0	0	1	0
1	0	0	0	x	0	0	0	0	0	0	1
unused					*any*	*legal*	*state*		x	x	x

Timing diagram:



Block Diagram: