Professor Fearing EECS150/Problem Set 5 Fall 2003

Due at 10 am, Fri. Oct. 10 in box outside 125 Cory Hall

Reading Ciletti: 8.2, 5.17, 9.7, Xilinx VirtexE p. 23-27, "Using Block SelectRAM"

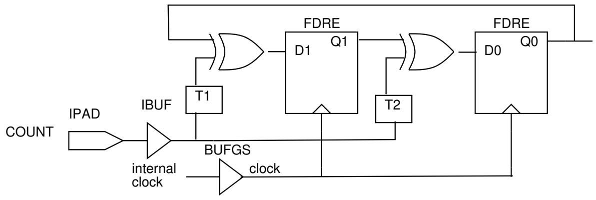
1. Synchronization (30 pts)

This question illustrates the potential problems caused by feeding asynchronous inputs into a FSM. (Even ignoring metastability). Consider the FSM below. The clock is connected using BUFGS so that there is negligible skew on the clock line. For this problem consider the parameters $T_{setup} = 0.8$ ns min, $T_{hold} = T_{CKI} = 0$ ns, $T_{CKO} < 1.4$ ns, and XOR plus interconnect (Q_1 to $D_0 = 4$ ns, Q_0 to $D_1 = 3$ ns). Delays are $T_1 = 8$ ns, and $T_2 = 6$ ns.

a. Determine the maximum clock speed using a timing diagram, showing clock, Q_0, D_1, Q_1, D_0.

b. Consider the clock signal running at 20 MHz. One of your colleagues has connected an unsynchronized input $COUNT$ to the FSM. Explain why this could be a bad idea by drawing a timing diagram, showing clock, $Q_0, D_1, Q_1, D_0, COUNT$. (I.e. show how setup time could be violated with COUNT being asserted at an inopportune time.)

c. An external system generates a high pulse on $COUNT$ lasting $50ns$. This pulse occurs at a random time (uniform distribution). Quantitatively estimate the chance of violating setup time on either FF.



2. FIFO Design (45 pts)

This problem considers the design of a FIFO (first in first out) register file using a **single port** block SelectRAM+ type RAM (fig. 32 in Xilinx VirtexE data sheet). The FIFO has 8 bits in and out $DIN[7:0]$ and $DOUT[7:0]$, synchronous inputs WR_EN, RD_EN, Reset, and CLK, and 2 outputs *Full* and *Empty*. The data path consists of the RAMB4_S8 512×8 RAM, an output register with clock enable, a detector for Full/Empty, and two synchronous 9 bit up counters with reset and count enable. Assume that synchronized inputs WR_EN, RD_EN, and DIN will be asserted for two periods of CLK, which may be overlapping. If FIFO is Full, ignore WR_EN, and in case FIFO is Empty, ignore RD_EN. (Assume FSMs communicating with FIFO will handle Full/Empty signals.)

a. Draw a detailed block diagram for the data path, carefully showing inputs and outputs.

b. Draw a functional timing diagram showing typical operation of the FIFO, including *Full* and *Empty*, and all control and data signals.

c. Draw an ASMD for the controller FSM for the FIFO.

3. Row Counter (25 pts)

Design a subsystem consisting of two counters ROW[7:0] and COLUMN[8:0] with a controlling FSM. On an input signal SOF initialize ROW to 0, then count up one for every input signal (SAV) to 8d'239, then halt until the next SOF. On input signal SAV, COLUMN is initialized to 0, then counts up one for every two clock cycles until reaching count 9d'319, then halt until next SAV. (Input signals are synchronized.)

a. Draw a detailed block diagram of the datapath showing all necessary control signals.

b. Draw ASMD for the control FSM.

c. Draw functional timing diagram near start and end of ROW and COLUMN counts.