Professor Fearing EECS150/Problem Set 7 Fall 2003

Due at 10 am, Fri. Oct. 24 in box outside 125 Cory Hall

(This problem set may be done individually or by a group of two people maximum. A group of two should hand in a single copy of the solution with both names affixed).

1. Video Decoder (30 pts)

Using `vid_dec.v` from the class web page:

a. Draw a detailed block diagram of the module, showing inputs, outputs, registers, counters, etc.

b. Draw an ASMD describing operation of this module.

c. Show with a timing diagram when valid video data is output on `DATA_OUT`.

2. Successive Approximation Design Example (45 pts)

You are given a black box containing combinational logic which takes an analog input V_{IN} and 8 binary inputs DAC[7:0]. The black box has a single digital output GREATER.H which is asserted if DAC[0:7]/128 (in volts) is greater than V_{IN}. (For example, if $V_{IN} = 1.2499$ volts, then GREATER would be asserted if $DAC > 160_{TEN}$.) Design a digital system, showing detailed block diagram, state diagram, and timing diagram, which outputs an 8 bit byte OUT[7:0] and strobe DONE.H as few cycles as possible after a START.H signal is received. (You may assume that V_{IN} is held constant until the DONE signal is asserted.) (Suggestion: do a binary search, starting with MSB. Hint: toggle flip flops.)

3. Vector Overlay Display (25 pts)

Draw a detailed block diagram for a module which can superimpose an 8×8 graphical vector representing motion direction onto a 240x320 digital video stream. There are 81 possible 8×8 bit maps, stored in a ROM, where Adr[2:0] addresses the column, Adr[5:3] addresses 1 of 8 rows, and Adr[12:6] addresses which vector icon to display. The motion direction vector comes from a 29x39 dual port RAM, and digital video data comes from an ITU 656 video encoder.