**Motivation**

- Learn to configure external SDRAM
- Write and read from external SDRAM
- To use FIFOs as buffers
- Design a memory controller
  - You will need this for the project
- Analyze retention time of SDRAMs

**Methodology (1)**

- Initialize and configure SDRAM
- Generate 32-bit pseudo random numbers into the FIFO
- After first 16 words start reading of FIFO and writing to SDRAM and start programmable timing ...
- Fill SDRAM and stop write operation

**Methodology (2)**

- ... after programmable delay expires, start reading SDRAM and filling read FIFO
- Use identical pn-generator to compare data from read FIFO with written data
- Count the errors and display on LEDs

**Theory of SDRAM (1)**

- SDRAM: Synchronous Dynamic RAM
- Dynamic RAM is large but slow
- Synchronous interface allows more bandwidth
- SDRAM Control can be tricky
Theory of SDRAM (2)
- DRAM is BIG so we time mux address
  - Row Address
  - Column Address
- Steps to Read/Write
  - Send Row Address
  - Send Column Address
  - Send/Get Data

Theory of SDRAM (3)
- SDRAM Steps to Read/Write
  - Send Row Address
  - Send Start Column Address
  - Send/Get Data
  - Send/Get Data
  - Send/Get Data

Theory of SDRAM (4)
- SDRAM is a large FSM
  - Send it a command
  - Get a response
- SDRAM Controllers Job:
  - Send the right command signals
  - Ensure command sequences are timed right

SDRAM Initialization

SDRAM Commands

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<tr>
<th>COMMAND</th>
<th>BUS Width</th>
<th>CAS/CR</th>
<th>OP CMD</th>
<th>ADDR</th>
<th>CYC</th>
<th>NOTES</th>
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Read Operation
Write Operation

Write Timing

Block Diagram

SDRAM

Controller (1)

SDRAM Controller (2)

FIFOs
LFSR
- Pseudo Random Sequences
- Signature Generation/Checking
- Built in Self Test (BIST)
- Pattern can be exactly repeated

The Checkpoint
- You have two weeks
  - First Week: Simulation
  - Second Week: Demo circuit on board
- START EARLY