Write behavioral Verilog for the following components:

- Carry Flip Flop
- Right Shift Register
- Full Adder
The D shifter is initialized to 4'b1000 when LdD is true. When the 1 shifts through to the output Cnt, it is a signal to the Control that four cycles of single bit addition have been executed.

The system works as follows. The Reset signal is asserted for exactly one clock period. On the first rising clock edge with Reset true, the Control enters the Initialize state and asserts the control signals Ld and Rst. On the next rising edge, with Ld and Rst true, the system loads A[3:0] into the A shifter, B[3:0] into the B shifter, 4'b1000 into the D shifter, and 0 into C.

At the same time, the system enters the Add state. Shortly after entering the Add state, A[0] and B[0] become visible to the adder’s inputs, with Cin = 0. After a further propagation delay, a single Sum bit S[0] and a new Cout are formed. With the control signal ShR set to true, the shifters are set to shift to the right on the next clock edge.

On this next edge, the shifters actually shift to the right. S shifts in the 0th sum bit and C receives the previous Cout. After a short delay, A[1] and B[1] appear at the shift right outputs of A and B, and the previous carry is now at Cin. After a further propagation delay, S[1] is formed with a new Cout.


Complete a sketch of the system’s timing using the diagram below as a start:

d. Write the Behavioral Verilog for the Control