Problem Set #8 (Assigned 26 October, Due 4 November)

SOLUTIONS

(i) Given the following datapath schematic, what are ALL of the architectural level register transfer operations (e.g., Reg ← Reg op Reg) that can be executed in a *single* processor cycle? The functional unit at the right of the datapath is a subtrator; at the left is an adder.

- R1 ← R0 + R3
- R2 ← R0 + R3
- R1 ← R0 + R2
- R2 ← R0 + R2
- R1 ← R1 + R2
- R2 ← R1 + R2
- R1 ← R1 + R3
- R2 ← R1 + R3
- R0 ← R1 – R2
- R3 ← R1 – R2
- R0 ← R1 – R0
- R3 ← R1 – R0
- R0 ← R3 – R2
- R3 ← R3 – R2
- R0 ← R3 – R0
- R3 ← R3 – R0

![Datapath Schematic](image-url)
(ii) Starting with the four registers and two functional units (ADD, SUB), design a bussing structure for the datapath so you can implement ANY register-to-register ADD or register-to-register SUB (including the same register used as both sources and the destination). It is never the case that both ADD and SUB take place at the same time. Your bussing design must use the fewest possible additional wires to accomplish this task.
(iii) Revise your solution to (ii) for the case where ADD and SUB can occur simultaneously, but never have the same target register (it wouldn’t make sense to write something into the same register from two different places at the same time!). Your design must use the fewest possible wires!