SDRAM Memory Controller

- Static RAM Technology
  - 6T Memory Cell
  - Memory Access Timing
- Dynamic RAM Technology
  - 1T Memory Cell
  - Memory Access Timing

Tri-State Gates

Slick Multiplexer Implementation

Basic Memory Subsystem Block Diagram

Static RAM Cell

Typical SRAM Organization: 16-word x 4-bit
Write Enable is usually active low (WE_L)
- Din and Dout are combined to save pins:
  - A new control signal, output enable (OE_L) is needed
  - WE_L is asserted (Low), OE_L is disasserted (High)
  - D serves as the data input pin
  - WE_L is disasserted (High), OE_L is asserted (Low)
  - D is the data output pin
  - Both WE_L and OE_L are asserted:
    - Result is unknown. Don’t do that!!!

Typical SRAM Timing

Problems with SRAM
- Six transistors use up lots of area
- Consider a “Zero” is stored in the cell:
  - Transistor N1 will try to pull “bit” to 0
  - Transistor P2 will try to pull “bit bar” to 1
- Bit lines are already precharged high: Are P1 and P2 really necessary?

1-Transistor Memory Cell (DRAM)
- Write:
  1. Drive bit line
  2. Select row
- Read:
  1. Precharge bit line to Vdd/2
  2. Select row
  3. Cell and bit line share charges
  4. Sense (fancy sense amp)
  5. Write: restore the value
- Refresh:
  1. Just do a dummy read to every cell

Classical DRAM Organization (Square)
- Square keeps the wires short:
  - Power and speed advantages
  - Less RC, faster precharge and discharge is faster access time!

DRAM Logical Organization (4 Mbit)
- Square root of bits per RAS/CAS
  - Row selects 1 row of 2048 bits from 2048 rows
  - Col selects 1 bit out of 2048 bits in such a row
Control Signals (RAS_L, CAS_L, WE_L, OE_L) are all active low
Din and Dout are combined (D)
WE_L is asserted (Low), OE_L is disasserted (High)
D serves as the data input pin
WE_L is disasserted (High), OE_L is asserted (Low)
D is the data output pin
Row and column addresses share the same pins (A)
RAS_L goes low: Pins A are latched in as row address
CAS_L goes low: Pins A are latched in as column address
RAS/CAS edge-sensitive

Every DRAM access begins at:
1. Assertion of the RAS_L
2. 2 ways to read: early or late v. CAS

DRAM Read Cycle Time

Early Read Sequencing
1. Assert Row Address
2. Assert RAS_L
   1. Commence read cycle
   2. Meet Row Addr setup time before RAS/hold time after RAS
3. Assert OE_L
4. Assert Col Address
5. Assert CAS_L
   1. Meet Col Addr setup time before CAS/hold time after CAS
   2. Valid Data Out after access time
6. Disassert OE_L, CAS_L, RAS_L to end cycle

Late Read Sequencing
1. Assert Row Address
2. Assert RAS_L
   1. Commence read cycle
   2. Meet Row Addr setup time before RAS/hold time after RAS
3. Assert CAS_L
   1. Meet Col Addr setup time before CAS/hold time after CAS
4. Assert OE_L
   1. Valid Data Out after access time
   2. Disassert OE_L, CAS_L, RAS_L to end cycle
Key DRAM Timing Parameters

- $t_{RAC}$: minimum time from RAS line falling to the valid data output.
  - Quoted as the speed of a DRAM
  - A fast 4Mb DRAM $t_{RAC} = 60$ ns
- $t_{RC}$: minimum time from the start of one row access to the start of the next.
  - $t_{RC} = 110$ ns for a 4Mbit DRAM with a $t_{RAC}$ of 60 ns
- $t_{CAC}$: minimum time from CAS line falling to valid data output.
  - 15 ns for a 4Mbit DRAM with a $t_{CAC}$ of 60 ns
- $t_{PC}$: minimum time from the start of one column access to the start of the next.
  - 35 ns for a 4Mbit DRAM with a $t_{PC}$ of 60 ns

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