1 Time Table

<table>
<thead>
<tr>
<th>ASSIGNED</th>
<th>Friday, October 3rd</th>
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<tbody>
<tr>
<td>DUE</td>
<td>Friday, October 10th</td>
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1. CLD2 Problems.
   (a) 4.3
   (b) 4.8
   (c) 4.10
   (d) 9.17
   (e) 9.18
   (f) 9.19

2. Find a copy of the ATF16V8B datasheet from Atmel.
   (a) What does the security fuse do?
   (b) What are the three different modes in which the chip can be operated? What are the maximum number of inputs, outputs, and flip flops in each mode?
   (c) What is the maximum number of product terms (implicants) that can be used in the next-state logic without using any combinational output blocks? What is the maximum number of literals per product term?
   (d) For the -10 parts, what is the worst-case delay from an input change to a non-registered output change? Registered output change? What does this say about the maximum frequency of an FSM implemented using this part?
   (e) What is the power consumption of the part at that frequency at 5 V and 25 C?

3. Implement the 163 counter from CLD2 figure 7.15 using a copy of the ATF16V8B logic diagram. Using another copy, implement as much as you can of the 8-bit counter in CLD2 figure 7.17.

4. How does the ATF16V8B compare to a Xilinx Virtex-II CLB in terms of the number of flip flops, and the complexity of the next-state logic for each flip flop?

5. Using a ROM and register to implement the FSMs in Problem 3, how many address bits would the ROM require and how many bits wide would the register need to be in each case?