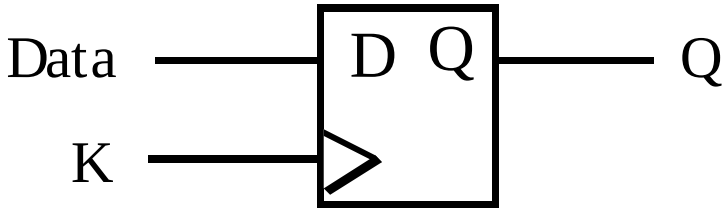


0 Admin
1 Recap
2 D FF timing
3 Toggle and JK FF

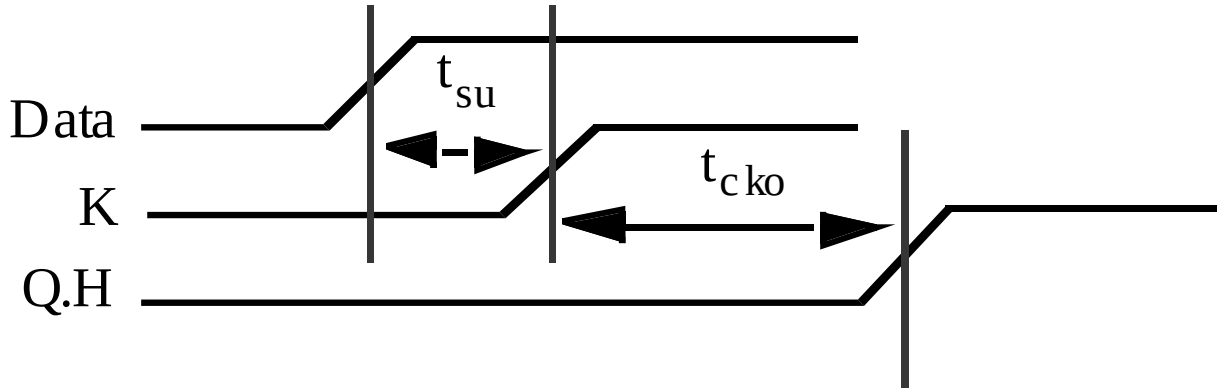
1 RECAP

- X74_163 synchronous counter
- FSM using counters

2 D FF Timing



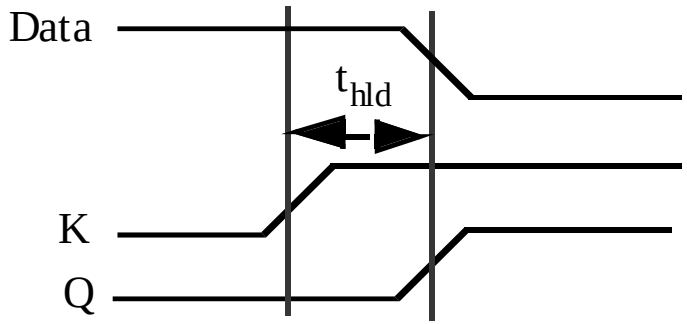
Setup time: min time before K for data to be valid



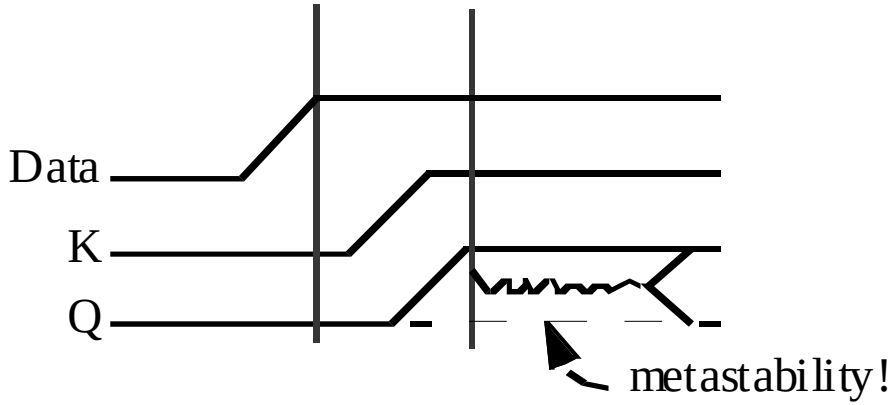
2 D FF Timing (cont.)

Hold Time

T_{hld} = min time after K for which data must remain valid

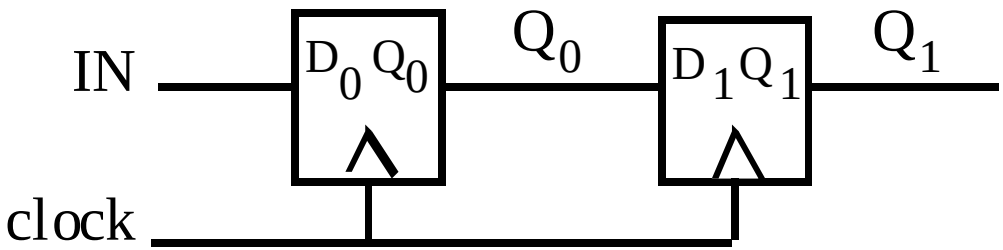


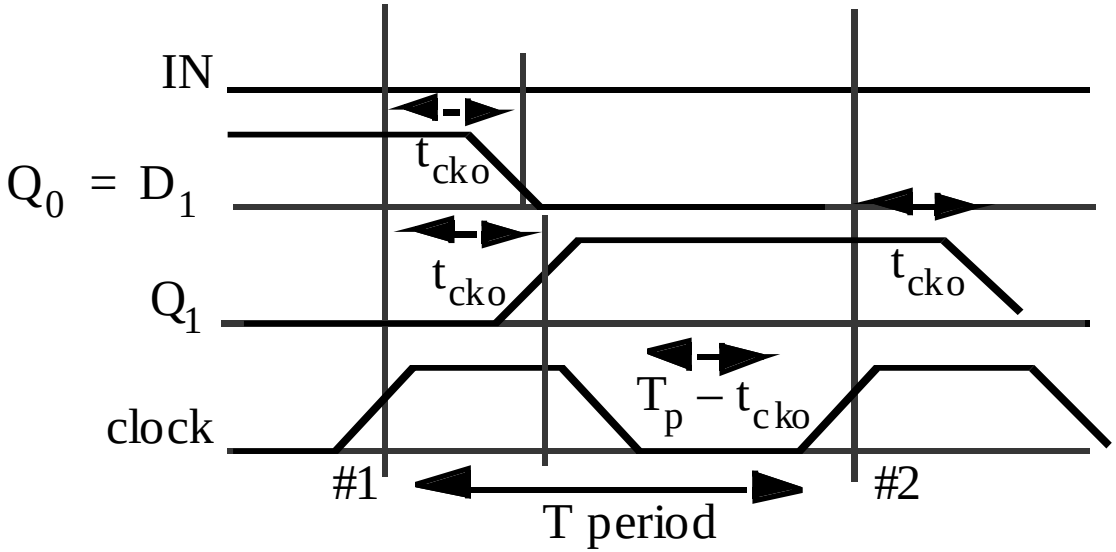
What happens if setup and/or hold is violated? Indeterminate



2 D FF TIMING (cont.)

2.1 Shift Register Revisited





2 D FF TIMING (cont.)

2.1.1 Timing Constraints for Shift Register

FF #0: If input = 0 all time, t_{su}, t_{hld} automatic

FF #1: constraint t_{su}: D_1 must be stable t_{su} before clock edge 2

$$\Rightarrow t_{period} - t_{ckomax} > t$$

constrain t_{hold}: D_1 must be stable for t_{hld} after clock edge 1

$$\Rightarrow t_{ckomin} > t_{hld}$$

2 D FF TIMING (cont.)

2.2 Xilinx Timing (4005-4)

Shift register holdtime 0 min

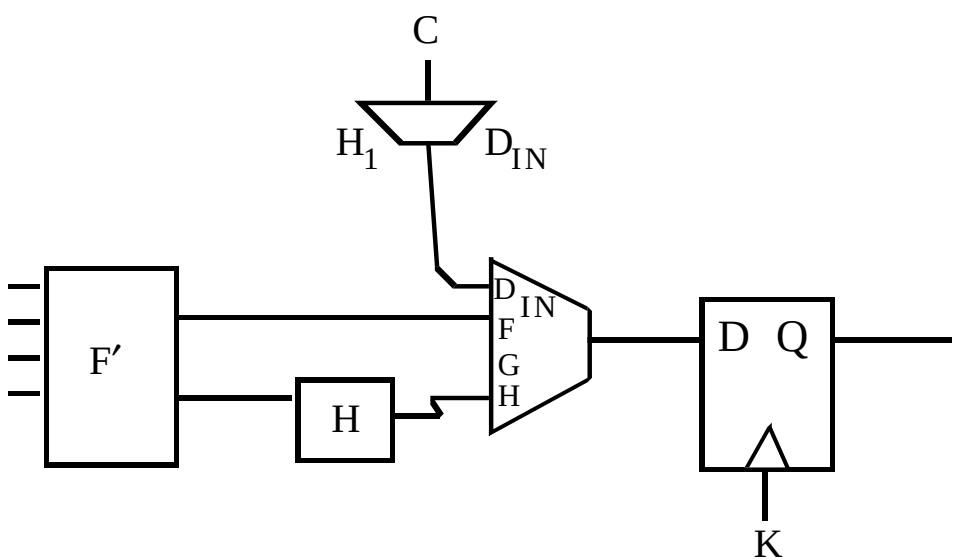
t_{cko} 3.7 ns

setup time D_{in}

t_{Dick} 3.0 ns

F´/G´ and H´

t_{IHCK} 6.1 ns



T_{hold} = 0, but watch out if clock skew

2 D FF TIMING (cont.)

2.2 Xilinx Timing (cont.)

How fast can it run?

$$\frac{1}{\text{min clock period}} = \frac{1}{t_{cko} + t_{setup}}$$

Depends on routing delay (non-deterministic)

Can use timing analyzer in XactStep

Example: 4-bit shift register: ~100 MHz clock (everything else is slower)

2 D FF TIMING (cont.)

2.3 Clock Skew

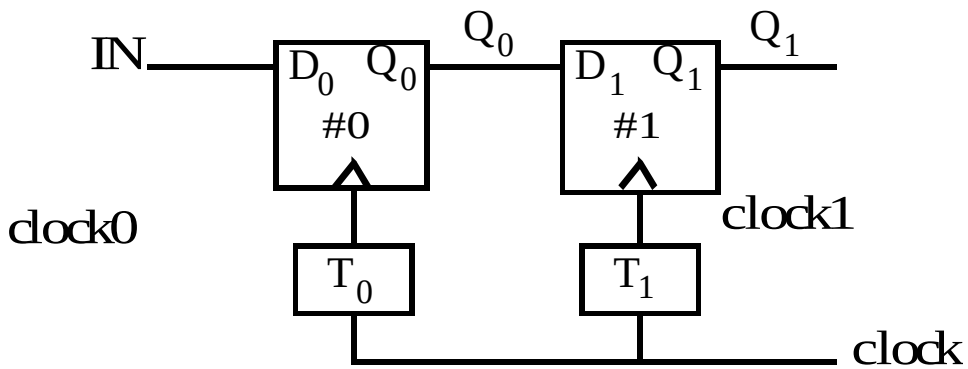
What is skew?

- Timing delays due to distance

$$(2\times10^8 \text{ m/s}) \quad 1\,\text{ns} = 0.2\,\text{m} \qquad \text{(off chip)}$$

- Clock distribution network on chip

See in shift register example

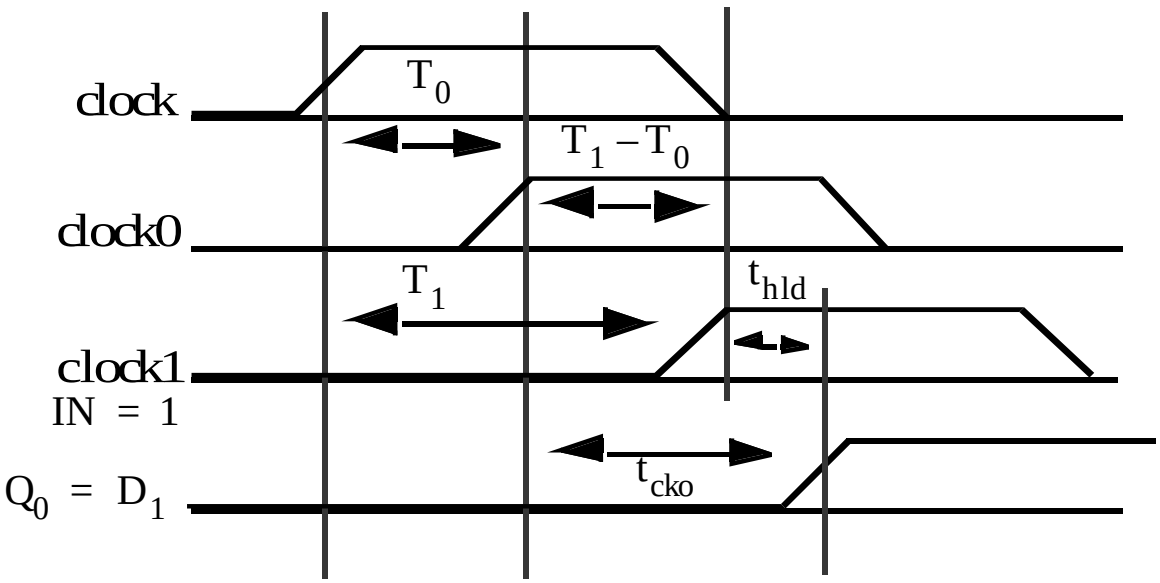


What is max ($T_0 - T_1$) for proper operation?

min ($T_0 - T_1$) for proper operation?

2 D FF TIMING (cont.)

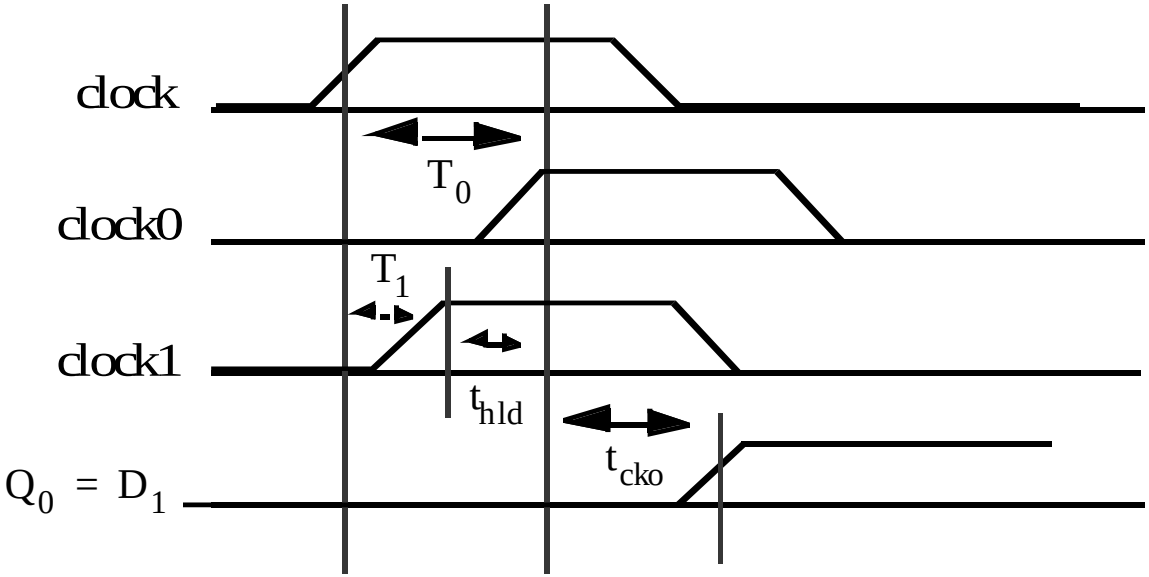
2.3 Clock Skew (cont.) – $T_1 > T_0$



Ok if $t_{cko} > T_1 - T_0 + t_{hld}$

2 D FF TIMING (cont.)

2.3 Clock Skew (cont.) – $T_1 < T_0$

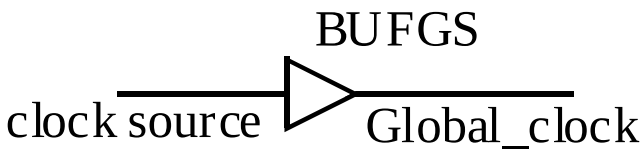


For $T_1 < T_0$, no problem due to clock skew

Ok if $T_0 + T_{cko} > T_1 + T_{hold}$

well designed logic $t_{cko} > T_{hold}$, and we are given $T_0 > T_1$.

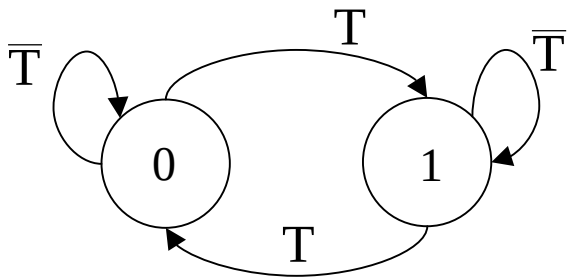
How to guarantee low clock skew? ~0.1 ns



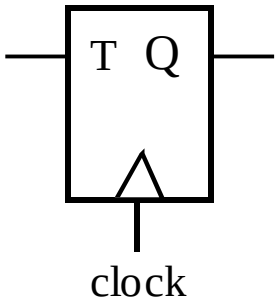
limit 4

3 OTHER FF TYPES

Toggle Flip Flop



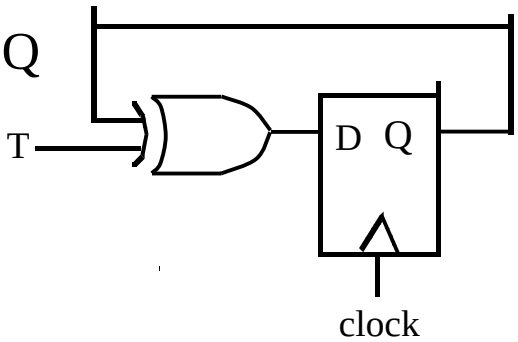
FTRSE



Convert D to T

T	PS	NS
0	0	0
0	1	1
1	0	1
1	1	0

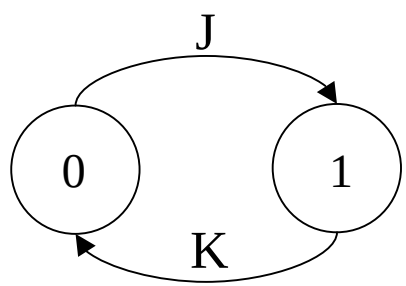
$D = T \oplus Q$

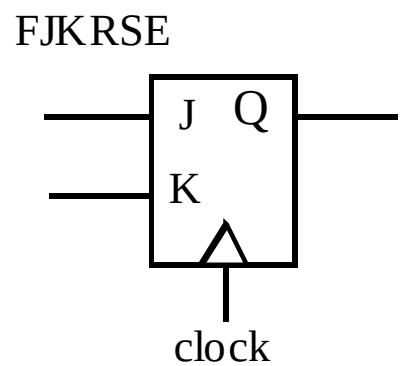


3 OTHER FF TYPES (cont.)

JK FF

J	K	Q_{n+1}	Comment
0	0	Q_n	hold
0	1	0	clear
1	0	1	set
1	1	$\overline{Q}_n$	toggle





Convert D to JK

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	X	0
1	0	X	1
1	1	0	1
1	1	1	0

$$D = \overline{J}\,\overline{K} \cdot Q_n + J\overline{K} \cdot \overline{Q}_n + J\overline{K}Q_n + JK\overline{Q}_n$$
$$= \overline{K}Q_n + J\overline{Q}_n$$