Homework #10

This homework is due on Friday April 26th by 1pm. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted.

All problems are based on the “List Processor Design Example” presented in class.

1. Draw the state transition diagram for the FSM controller for architecture #4. Exactly how many clock cycles are needed to process a list with n nodes?

2. For the timing analysis, we assumed that the data-path registers did not have a reset input. Now, assume that the registers do have resets, but otherwise have the same delay characteristics. What would be the new maximum clock frequency for the optimized design of architecture #4?

3. Assume that we are allowed to restrict nodes to be aligned on multiples of 2 bytes. Redraw the new simplified data-path of architecture #4 to take advantage of this restriction. Rewrite the RTL description of the algorithm. Draw the associated FSM controller state transition diagram.

4. Now assume that we can restrict nodes to be aligned on multiples of 2 bytes and we can use a memory with a 16-bit wide output. Again redraw the new simplified data-path of architecture #4. Rewrite the RTL description of the algorithm. Draw the associated FSM controller state transition diagram.