1. Flip-flops and timing.

a) For the circuit shown, assume that all the flip-flops initially hold logic 0. Draw the waveform that appears at point $y$.

b) Assume the flip-flop setup time is 75ps and its clock-to-Q delay is 100ps. If the mux propagation delay is 150ps, what is the maximum clock frequency for this circuit?
2. Logic gate timing waveforms.

Below is shown the waveforms corresponding to a low-to-high and a high-to-low transition for an inverter. Draw approximate transition waveforms for the other situations shown below. Assume that all transistors in all the gates and inverters are of the same strength.

a) $V_x$ initially is high, set $a = b = \text{high}.$

b) $V_x$ initially is low, set $a = \text{high}$, $b = \text{low}$

c) $V_x$ initially is low, set $a = b = \text{low}.$
d) Show both transitions.

![Diagram of CMOS AND gate with NAND gate followed by inverter]

3. **Gate delay.**

Consider a CMOS AND gate constructed as a NAND gate followed by an inverter.

Assume the inverter propagation delay is expressed as follows:

\[ \tau_p = 50 + 100 \cdot f \]

where \( f \) is the fanout of the inverter, expressed in number of transistor-gate inputs (inverters contribute 2 to \( f \), one input of 2-input gates contribute 2,). Assume this inverter has the same propagation delay for both low-to-high and high-to-low transitions.

The NAND gate propagation delay is expressed as:

\[ \tau_{PLH} = 100 + 75 \cdot f \]
\[ \tau_{PHL} = 100 + 125 \cdot f \]

For the low-to-high and high-to-low transitions, respectively. Write expressions for the propagation delay of the AND gate:

\[ \tau_{PLH} = \]
\[ \tau_{PHL} = \]
4. **Power/energy units.**

   a) Consider a logic gate driving an output with an average of one transition per eight clock cycles (clock frequency is 100MHz). The output has a total capacitance of 10fF, and Vdd=3volts. What is the average power consumption of the gate?

   b) Battery storage is often expressed in Watt-hours. What is the energy storage capacity in Joules of a 10 Watt-hour battery? How long would it power the above gate?

5. **Switching power.**

   Consider the simple AND/OR circuit shown below. New values are applied to the four inputs at a rate of \( f \). Input values are applied as independent uniform random sequences to each of the four inputs; i.e., for each input, on each appearance of a new input, \( \text{Prob}(1)=\text{Prob}(0)=1/2 \). Write an expression for the average power consumed by gate 1 in terms of \( f \) and the switching energy \( E_{sw} \). Do the same for gate 3.
6. Power and voltage scaling.

To first approximation, under a limited voltage range, a reduction in power supply voltage (Vdd) in MOS circuits results in a linear increase in gate delay and thus maximum clock rate. This fact is often used to reduce power consumption in cases where a reduction in performance can be tolerated, or compensated for in another way.

Consider a special processor inside a car engine, whose job is to control the fuel air mixture to the injectors. Let’s assume that the processor must make 100 adjustments per second and it takes 5K operations for each adjustment. Assume that we chose to use a processor that has peak performance of 1M operations/sec and at that rate uses 1Watt. Your boss tells you that 1 Watt is too much. Without changing the supply voltage, is there a way to reduce the power consumption? If so, by how much? Is there a way to reduce the power consumption even more by lowering the supply voltage? If so, what voltage level would you use and what would be the resulting power?