Homework #5

This homework is due on Friday March 1st by 1pm. Homework will be accepted in the EECS150 box on the door to room 218 Cory Hall. Late homework will be penalized by 50%. No late homework will be accepted after the solution is posted.

1. From Mano: Problem 5-17.
   a) Design the circuit described in the exercise,
   b) Write the behavioral Verilog description of the circuit based on your state transition diagram (similar to the lab exercise),
   c) Write the structured Verilog description of the detailed circuit you derived in part a) using low-level gates for the combinational logic and implied flip-flop(s) for the state register. Write three modules – the combinational logic, the state register, and the composition of the two as the FSM.

   Hint for part a): The method for generating 2’s complement is not the usual method of inverting all the bits and adding one. You can discover an alternate method by looking at several simple examples of binary numbers and their respective 2’s complement representation. Note where the bits are the same and where they are different.