

University of California at Berkeley
EECS Department

CS 150
Spring 2002

J. Wawrzynek
Project Info.

Final Project Grading

This document has information that you will need to know to receive credit for you project, including extra credit information.

1 Introduction

Your project grade will be based on information derived from the following sources:

- Submitted Verilog source code.
- Final project demonstration.
- Your online report.

2 Verilog Code

Your Verilog code will be our main source to determine of the quality of your design. It is very important that we understand the detailed operation of your circuit. Therefore, to help us understand your design you will need to comment your code. Put a comment block for every module definition, comments to identify the important registers and wires, and additional comments in the body of the module in non-obvious spots to help us understand your intent. We will use your code along with some specific questions asked in person during your demonstration or in the online report.

Someone not familiar with your project should be able to understand how your circuit works from reading the project specifications handout and then your Verilog source code.

3 Demonstration

Project demonstrations will take place the last full week of classes (5/6–5/10). All lab sections will meet as scheduled. **You must demonstrate your project during your normally scheduled lab section.** Both partners must be present for the demonstration. There will be no make-up time for demonstrations except in the case of medical emergencies.

During your lab section the week before demo week you must sign up for a demonstration time slot. See your TA for Sign-up sheets. At the beginning of your lab section during

demo week, if we do not find your name on the list, we will assume that you have given up on the project and will receive a 0 grade.

During your demonstration we will ask you to compile your Verilog source code and generate a Xilinx “bits” file for your project. This “bits” file will be the one that you must use to demonstrate your project.

It is very important that you have something working at the demonstration. If you decide to make last minute changes before the demonstration, be certain to save away a copy of a working version of your project. That way, if something goes wrong at the last moment, you will still have something to show. And remember, a working project that does not meet all the specs is worth more than a project that meets all the specs but doesn't work!

Get to the lab well before your demo time to get things setup. If you are not ready when your time slot comes up, we will be forced to move on to the next group, and you will not get credit for a demonstration.

During the demonstration we will ask you questions about your design, then test it automatically from a computer program that sends MIDI commands stored in a file to the USB port. You will not have advanced access to our actual tests, but you will have access to the program for sending MIDI commands. If you would like to use it to test your project on your own, ask your TA about it.

Cheating. We will take a copy of your Verilog source code for later inspection. We will also later run your Verilog source code through an anti-cheating program that will compare it to the Verilog source code files from other groups. Remember, you must turn in your own work. We will be tolerant of your “borrowing” small pieces of design from other groups, as long as you give them credit. If you copy without assigning appropriate credit, we will consider that you have cheated and take appropriate steps (0 grade on the project and turn you over to the Office of Student Judicial Affairs). If you copy too much from other groups, even when having given them credit, we will reduce your grade. If you have any doubts about this policy, please ask Prof. Wawrzynek.

4 Final Report

You are not required to turn in a lengthy written report, however, you must submit a short online report by filling out the form linked to the class webpage. The form must be completed before your project demonstration. Consider the questions carefully, and please don't do it at the last minute.

While it is not a formal report, it is still important that you write clearly, are well organized, and use correct grammar. Make sure to proofread your report and correct mistakes before you turn it in.

Part of the online report are questions about division of labor and who did what. If you feel that there was a strong imbalance in your group and do not feel comfortable reporting it online, please send email to Prof. Wawrzynek.

5 Project Grading

Your project grade will be based on its functionality and its organization. Functionality addresses the project's ability to perform according to the project specification. Deductions will be made for missing functions or incorrect behavior under some inputs. If your project is not fully functional we will evaluate it based on whatever function can be demonstrated, along the lines of the checkpoints.

The organization of your design addresses the structure of your circuits and their efficiency. Using many more LUTs and Flipflops than are necessary is considered poor organization and will result in deductions. Deductions will also be made for confusing, hard to understand circuit structures. You should strive for simple circuits and simple Verilog descriptions.

5.1 Extra Credit

No extra credit will be given to projects not meeting the minimal requirements.

Extra credit tasks with their associated percentage points are listed below. The percentages correspond to points based on the total maximum project score (not the actual score you receive). You can receive full extra credit points for one task and only partial points for additional ones. The formula is as follows:

$$\text{extra credit points} = \text{task}_a \text{ points} + 0.5 \text{ task}_b \text{ points} + 0.25 \text{ task}_c \text{ points} + \dots$$

We will choose task_a to be your task with the most points, task_b to be your task with the second most points, etc., to maximize your total extra credit. Extra credit will be added to your final course grade after all grading is complete and the grade curve computed.

<i>task</i>	<i>points</i>	<i>description</i>
early check-off	8	Basic project check-off during makeup lab Friday 4/26, 3pm. Other extra credit tasks may be checked off later.
two instruments	5	Monophonic synthesizer with two different instruments. Use "channel" field in MIDI command to select instrument.
two-voice polyphony	10	Synthesizer capable of playing two voices simultaneously.
> two-voice polyphony	15	Synth. capable of playing more than two voices simultaneously.
linear interpolation	15	As described in project specification handout.
low 4-LUT count	10	Basic project implemented with no more than 260 4-LUTS.

6 Kit Turn-in

Your last job will be to disassemble you project and return the parts along with the rest of your lab kit. **You must remove the wire wrap wires and wrap-ids from your FPGA board before you turn it in.** Do this carefully!

Return you lab kit to 125 Cory the week of 5/20. We will announce the times later.