A simple processor takes input from one memory and writes its result to another, as shown below:

MEM1 supplies a 64-bit data item every 10ns, and MEM2 can accept a new 16-bit item every 10ns. Data in MEM1 is organized in groups of four 16-bit words, \{a,b,c,d\}. Your processor must form \( y = a + b + c + d \). Assume that you have 16-bit adders with a delay of 10ns and registers with \( T_{\text{SETUP}}=0.5\)ns and \( T_{\text{CLK}}\rightarrow Q=0.5 \). Your job is to design the processor data-path that can supply a new \( y \) value to MEM2 every 12ns, while minimizing the cost. Draw your data-path below. You do not need to show the controller.