For this problem assume that your complete library of logic components comprises 2-input AND, OR, and XOR gates and inverters. Assume that inverters have cost of one unit and delay of one unit, and all other logic gates have cost of 2 units and delay of 2 units (ignore fanout and wire delay). With these assumptions, a 2-input mux could be implemented with two AND gates, one OR gate, and one inverter, and would cost 7 and have delay 5 from the select input to output and a delay of 4 from data input to output.

Consider the structure of a 12-bit carry-select adder with inputs a[11:0], b[11:0], cin, and outputs s[11:0], cout. It has the blocks sizes, 3,4,5, starting from the least significant side (the right). All “sub-adders” are carry-ripple adders. Assume that each ripple adders is made up only of full-adder cells (one-bit adders).

Full adder (FA):

Cost: 4 units
Delay $a/b \rightarrow S = 4$
Delay Cin $\rightarrow S = 2$

Cost: 8 units
Delay $a/b \rightarrow Cout = 6$
Delay Cin $\rightarrow Cout = 4$

Total Cost: 12 units
a) Calculate the total cost for the 12-bit carry-select adder:

\[
\text{Total Cost} = (11 \text{ Muxes} \times 7) + (21 \text{ FA} \times 12) \\
= 77 + 252 \\
= \text{329 units}
\]

b) Calculate the delay from Cin to Cout:

\[
\text{Delay from Cin to Cout} = 12 + 5 + 5 \\
= \text{22 units}
\]

c) In words, describe the path with the worst case delay from any of the inputs to any of the outputs:

Note that all blocks run in parallel. The carry out of the 4-bit ripple adder comes at time of 18 units (a4/b4 → Cout5 = 6 units, then 3 stages of Cin → Cout), is delayed by 4 by the first carry mux, and is then used by select of final carry mux, which adds 5 delay units. So the total delay is 27 units.