EECS150 - Digital Design
Lecture 2 - CMOS

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Outline

• Overview of Physical Implementations
• CMOS devices
• Announcements/Break
• CMOS transistor circuits
  – basic logic gates
  – tri-state buffers
  – flip-flops
    • flip-flop timing basics
    • example use
    • circuits
Overview of Physical Implementations

_The stuff out of which we make systems._

- Integrated Circuits (ICs)
  - Combinational logic circuits, memory elements, analog interfaces.
- Printed Circuits (PC) boards
  - substrate for ICs and interconnection, distribution of CLK, Vdd, and GND signals, heat dissipation.
- Power Supplies
  - Converts line AC voltage to regulated DC low voltage levels.
- Chassis (rack, card case, ...)
  - holds boards, power supply, provides physical interface to user or other systems.
- Connectors and Cables.
Integrated Circuits

- Primarily Crystalline Silicon
- 1mm - 25mm on a side
- 100 - 200M transistors
- (25 - 50M “logic gates”)
- 3 - 10 conductive layers
- 2002 - feature size $\sim 0.13\text{um} = 0.13 \times 10^{-6} \text{ m}$
- “CMOS” most common - complementary metal oxide semiconductor

Chip in Package

- Package provides:
  - spreading of chip-level signal paths to board-level
  - heat dissipation.
- Ceramic or plastic with gold wires.
Printed Circuit Boards

- fiberglass or ceramic
- 1-20 conductive layers
- 1-20in on a side
- IC packages are soldered down.

Multichip Modules (MCMs)

- Multiple chips directly connected to a substrate. (silicon, ceramic, plastic, fiberglass) without chip packages.
Integrated Circuits

- Moore’s Law has fueled innovation for the last 3 decades.

- “Number of transistors on a die doubles every 18 months.”
- What are the side effects of Moore’s law?
Integrated Circuits

• Uses for digital IC technology today:
  – standard microprocessors
    • used in desktop PCs, and embedded applications
    • simple system design (mostly software development)
  – memory chips (DRAM, SRAM)
  – application specific ICs (ASICs)
    • custom designed to match particular application
    • can be optimized for low-power, low-cost, high-performance
    • high-design cost / relatively low manufacturing cost
  – field programmable logic devices (FPGAs, CPLDs)
    • customized to particular application after fabrication
    • short time to market
    • relatively high part cost
  – standardized low-density components
    • still manufactured for compatibility with older system designs
CMOS Devices

- MOSFET (Metal Oxide Semiconductor Field Effect Transistor).

**Top View**

**Cross Section**

The gate acts like a capacitor. A high voltage on the gate attracts charge into the channel. If a voltage exists between the source and drain a current will flow. In its simplest approximation the device acts like a switch.

**nFET**

\[ V_{gs} = '0' \]

\[
\begin{array}{c}
\text{S} \\
\hline
\text{G} \\
\hline
\text{D} \\
\end{array}
\]

**pFET**

\[ V_{gs} = '1' \]

\[
\begin{array}{c}
\text{S} \\
\hline
\text{G} \\
\hline
\text{D} \\
\end{array}
\]
Announcements

If you are on the wait list and would like to get into the class you must:

- Turn in an appeal for on third floor Soda
- Attend lectures and do the homework, the first two weeks.
- In the second week of classes, go to the lab section in which you wish to enroll. Give the TA your name and student ID.
- Later, we will process the waitlist based on these requests, and lab section openings.
Announcements

◆ Reading assignment for this week.
  ◆ All of chapter 1
  ◆ Chapter 10 sections 1,2,7,8,9

◆ Homework due next Thursday before class. Will be posted later today.

◆ Questions about class policy etc. covered on Tuesday?
Transistor-level Logic Circuits

- Inverter (NOT gate):

- NAND gate

- Note:
  - out = 0 iff both a AND b = 1
  - therefore out = (ab)'
  - pFET network and nFET network are duals of one another.

How about AND gate?
Transistor-level Logic Circuits

Simple rule for wiring up MOSFETs:

- nFET is used only to pass logic zero.
- pFet is used only to pass logic one.
- For example, NAND gate:

Note: This rule is sometimes violated by expert designers under special conditions.
Transistor-level Logic Circuits

• NAND gate

• NOR gate

• Note:
  – out = 0 iff both a OR b = 1 therefore out = (a+b)’
  – Again pFET network and nFET network are duals of one another.
  – Other more complex functions are possible. Ex: out = (a+bc)’
Transistor-level Logic Circuits

- **Tri-state Buffer**

  \[
  \begin{array}{c|c|c}
  \text{OE} & \text{IN} & \text{OUT} \\
  \hline
  0 & 0 & Z \\
  0 & 1 & Z \\
  1 & 0 & 0 \\
  1 & 1 & 1 \\
  \end{array}
  \]

  "high impedance"
  (output disconnected)

- **Variations**

  Inverting buffer
  \[
  \begin{array}{c|c|c}
  \text{OE} & \text{IN} & \text{OUT} \\
  \hline
  0 & 0 & Z \\
  1 & 0 & 1 \\
  1 & 1 & 0 \\
  \end{array}
  \]

  Inverted enable
  \[
  \begin{array}{c|c|c}
  \text{OE} & \text{IN} & \text{OUT} \\
  \hline
  0 & 0 & 0 \\
  0 & 1 & 1 \\
  1 & - & Z \\
  \end{array}
  \]

  "transmission gate"

*Tri-state buffers are used when multiple circuits all connect to a common bus. Only one circuit at a time is allowed to drive the bus. All others “disconnect”.*
Transmission Gate

- Transmission gates are the way to build “switches” in CMOS.
- Both transistor types are needed:
  - nFET to pass zeros.
  - pFET to pass ones.
- The transmission gate is bi-directional (unlike logic gates and tri-state buffers).
- Functionally it is similar to the tri-state buffer, but does not connect to Vdd and GND, so must be combined with logic gates or buffers.
Transistor-level Logic Circuits

- Multiplexor

If $s=1$ then $c=a$ else $c=b$

- Transistor Circuit for inverting multiplexor:
**D-type edge-triggered flip-flop**

- The edge of the clock is used to sample the "D" input & send it to "Q" (positive edge triggering).
  - At all other times the output Q is independent of the input D (just stores previously sampled value).
  - The input must be stable for a short time before the clock edge.

![Diagram of D-type edge-triggered flip-flop](image-url)
Parallel to Serial Converter Example

- **Operation:**
  - Cycle 1: load $x$, output $x_0$
  - Cycle $i$: output $x_i$

- Each stage:

- 4-bit version:

```plaintext
LD  X = [x_{n-1}, x_{n-2}, ..., x_1, x_0]

P/S converter   out
clk

LD
xi
1
0
FF
clk

if LD=1
load FF from $x_i$
else from previous stage.

LD
x3
x2
x1
x0

out

clk

FF
FF
FF
FF
0
0
0
0

FF
FF
FF
FF
1
1
1
1
```
Parallel to Serial Converter Example

- timing:

\[ \text{clk} \]
\[ \text{LD} \]
\[ \text{out} \]
Transistor-level Logic Circuits

- Positive Level-sensitive latch
  ![Positive Level-sensitive latch diagram]

- Transistor Level
  ![Transistor Level diagram]

- Positive Edge-triggered flip-flop built from two level-sensitive latches:
  ![Flip-flop diagram]